TITOLO TESI

Sviluppo di un sistema di radiologia digitale basato su rivelatore a pixel con acquisizione single-photon counting

Presentata da: dott. dr. MARZEDDU Roberto
Coordinatore Dottorato: prof. BURDERI Luciano
Relatore: prof. RANDACCIO Paolo
Design of a x-ray imaging system based on an hybrid pixel working in single-photon counting mode
Abstract

This thesis describes the design and development of a digital imaging system for CT applications. It was designed to cope with a pixel hybrid detector based on the Medipix2 ASIC, which offer 2.8 cm x 2.8 cm sensitive area segmented in 262144 (512 x512) square pixels of 55 μm side length. Such a detector works in photon counting mode and can be coupled with different semiconductor sensor (e.g., silicon, gallium arsenide, cadmium telluride) to fit the specific application requirements.

The imaging system, named PPC (...), is composed on several custom designed cards and exploits a fast optical link and a PCI interface card to control the detector stage by means of an host personal computer. The minimum achievable acquisition rate is 25 frame/s with 10% of dead time.

A general overview of semiconductor detectors and in particular the Medipix2 hybrid detector are discussed as introduction to the PPC system description and characterization.

The conclusion outlines the current status of development and the obtained results.
Acknowledgements

I would like to thanks prof. Paolo Randaccio which helped me to start this challenging work on digital detectors since my graduate thesis. Thanks to INFN too for its financial support of the projects involved.
Table of contents
Introduction

At present, the market offers of-the-shell radiography devices for different applications. Beside commercial available devices, research group all over the world are studying new and even more performance detector.

The Medipix2 collaboration (CERN) has developed an advanced readout chip that combined with a pixellated semiconductor sensor can give an hybrid x-ray detector for x-ray imaging. The characteristic of such a detector is that it works in single-photon counting mode that is it counts the number of those photons which deposit, on the converting medium, an amount of energy greater than a minimum threshold or included between two thresholds. Such a detector offers low noise images, with high contrast and high spatial resolution.

This thesis relates about the design, building and test of a x-ray imaging system, based on the Medipix2 detector, which can be exploited to study an compare single-photon counting device whit integrating ones in the field of Computed Tomography applications.

This work has been accomplished in the framework of Medipix2 collaboration and in the behalf of the PPC first and the Breast-CT projects, funded by the Italian National Institute for Nuclear Research (I.N.F.N.).

This thesis summarizes the design and characterization of a digital imaging system for CT applications based on X-ray imaging detector with a square pixel size of 55 µm organized as a matrix of 512 x 512 pixels. Such a detector is made of a segmented Silicon sensor coupled with a readout ASIC named Medipix2.

A description of the contents of the thesis, chapter by chapter, follows:

- **Chapter 1**: Different detector technologies are overviewed. Emphasis is placed on the distinction between direct and indirect detection systems and integrating and counting methods. A advantages of digital imaging systems compared to analog systems and the potential of the direct detection photon counting hybrid pixel chips are summarized.
Chapter 2: After an overview of the available chip carriers and readout system for Medipix2, the Medipix2 pixel cell and the chip periphery architecture are described. The Medipixpix2MXR20 chip, an upgraded release of Medipix2 chip, is also considered. Finally, the chip operation protocols are explained.

Chapter 3: The development of the PPC imaging system is reported. The design constraints and the hardware of the single part composing the acquisition chain are discussed. The software application developed to control the system is illustrated.

Chapter 4: In this chapter the high- and low-level communication protocols of the PPC system are described in detail. The first electrical characterisations of the system are reported showing that the DAQ performs according to the design specifications.

Thesis summary: This final chapter deals with the conclusions which can be drawn from this work. The main results and their significance are discussed.
Chapter 1:

X-ray Imaging Devices

Abstract - Many different types of image receptor can be used in modern diagnostic radiology. Although most of the images in radiology are still only available on film which means in analog form the last decade has seen the emergence of a new generation of solid-state digital radiography (DR) detectors with the goal to improve the image quality and reduce the survey dose. Some of them are currently used in clinical applications beside or instead the conventional screen-film devices.

In this chapter a selection of medical X-ray imaging systems is considered with the aim to underline their intrinsic features and limits. Both commercially-available and novel technologies will be considered.

Photograph of the shadow of a concealed wire winding on a wooden bobbin (Röntgen 1895). This is one of the first pictures sent by Röntgen on 1st January 1896 to Sir Arthur Schuster, Professor of Physics in the University of Manchester (figure taken from R.F. Mould, Phys. Med. Biol. 40 (1995) 1741-1787).
1 X-ray imaging devices

For many years, screen-film (S/R) systems have been used almost exclusively for x-ray detection and image recording in conventional x-ray projection imaging. Indeed S/R features high efficiency and good quality images for most of the clinical applications but are also intrinsically limited by the restricted exposure latitude, time consuming developing process and absence of image post-processing [Mon05].

Although most of the images in radiology are still only available on film which means in analog form, in the past two decades, various digital radiography techniques have been developed with the aim to improve the image quality and reduce the survey-associated dose.

In this chapter a selection of medical X-ray imaging systems is considered with the aim to underline their intrinsic features and limits. Even if the future of radiography will be digital, analog film-based receptor will be described for first to underline their intrinsic limitations with respect to digital devices.

1.1 Classification criteria of imaging detectors

Imaging devices can be classified depending on their different properties about photon recording methods and architecture concepts.

1.1.1 Analog and digital detectors

Analog receptors (e.g., film-based receptor, image plate) attempts to reproduce the photon attenuation pattern (i.e., the radiograph) faithfully on a spatially continuous fashion. If the x-ray flux is enough also the signal intensity will appear to be continuous. In a digital imaging system, at some stage, the x-ray transmission pattern is sampled both in the spatial and intensity dimensions. In the spatial dimension, samples are obtained as averages of the intensity over picture elements or pixels. These are generally square areas, which are spaced at equal intervals (pitch) throughout the plane of the image. In the intensity dimension, the signal is binned
into one of a finite number of levels. This is normally equal to $2^n$ where the value of $n$ is designated as the number of bits to which the image is digitized. Intensity values of the digital image can, therefore, only take on discrete values, and information regarding intermediate intensities and variations on a sub-pixel scale is lost in the digitization process [Yaf97]. Due to the sampling theorem, the spatial resolution of a pixel detector is intrinsically limited by its Nyquist’s frequency defined as $1 / 2d$, $d$ being the pitch of the pixels. When the pixel size is larger than 2 times the detail size this will lead to image distortions called “aliasing”. The small pitch, however, not only provides a good spatial resolution but also confronts the pixel electronics with the problem of significant charge sharing between adjacent pixels. Charge sharing consists in the diffusion of the produced charge cloud during the collection process.

1.1.2 Direct and indirect photon conversion

This classification corresponds to different way of converting x-ray into a detectable signals. In direct conversion detectors, the X-ray are absorbed by a semiconductor or gas sensor and directly converted into electric charges. Indirect conversion detectors add an intermediate process; first, x-ray are adsorbed into a scintillator layer and converted into lower frequency light, which is in turn converted into electric charge by a photodiodes array. Usually direct photon detection is preferable for spatial and contrast resolution. The spatial resolution of indirect conversion detector is deteriorated because of the lateral spread of the light photons which is a function of the distance of the light emission point to the detector pads. It imposes a trade off between the absorption efficiency, related to the thickness of the scintillator layer, and the resolution properties.

1.1.3 Hybrid and monolithic architecture

This classification property is related to previous one. In monolithic detectors converting material is integrated with the electronics circuitry onto the same substrate while in hybrid devices the electronic circuitry and the sensor are processed separately (fig. 1.1). Monolithic devices are more robust and thinner compared to the hybrid ones but sometimes they should exploits non standard
processing technique to integrate the electronic components (made of low-resistivity silicon). On the other side, the main advantage of hybrid detectors is that the same readout chip can be combined with different sensors made of different materials, thickness and pixel shapes and sizes. The readout chip functionality can be adapted to a specific imaging task, and fundamental limits are only set by the CMOS component size which decreases steadily and by the performance of the sensor material.

![Schematic view of the hybrid concept, consisting of the sensor layer bump bonded to the readout chip. The sensor and electronic chip are both segmented in a bi-dimensional pixel array.](image)

**1.1.4 “Integrating” and “photon counting” acquisition mode**

This classification refers to the different principles for recording the signals from particles or photons. The photon counting acquisition method the signal height from a photon is compared to a threshold set in a comparator. If the signal exceeds this threshold the value of a counter is incremented. Each photon with an energy above threshold has the same weight of one. The possibility to set a threshold implies that background can be eliminated which increases the signal-to-noise ratio and the dynamic range.

The integrating acquisition method does not comprise a threshold. All the incoming signals including noise are added up. This reduces the signal-to-noise ratio (SNR) and the dynamic range. Moreover, a weighting of photons with different energies takes place. Photons of higher energy deposit more charge in the detector or produce more blackening which results in a higher signal. Compared to photon counting this could be a disadvantage. Usually the higher part of the x-ray spectrum
after having passed through the patient carries much less useful information than the lower energy part, but has more weight in the image formation of an integrating system. Examples for integrating systems are all kinds of film systems, flat panels and CCDs.

In photo counting approach each photon is individually processed so at conceptual level, it seems most adequate to detect photons due to the fact that the X-ray flux itself is already quantized. The main advantages of this approach can be summarized as follows:

- The information is digitized at pixel level so only the number of photons detected by each pixel is stored and read out. Therefore typical CCD side-effects like blooming, cross-talk between adjacent pixels or read-out errors due to incomplete charge transfer cannot occur.

- By applying a threshold to the charge signal coming from the sensor layer the dark current can be discarded and therefore low rate imaging can be performed. Moreover the energy threshold can reduce the Compton scattered events which are one cause why small details and low contrast objects are often undetectable. This effects is effective especially when mono-energetic X-ray sources are exploited.

- When more than one threshold and counter are implemented in every pixel, spectroscopic data can be gained improving the image quality.

- The maximum dynamic range achievable is only limited by the available counter depth in each pixel. Thus over-exposed bright regions in an overall rather dark image and vice versa pose no longer an insolvable problem.

- The detector exhibits a perfectly linear response over the whole exposure range.

The problem of charge sharing is especially critical for counting systems since it leads to the omission of events and to a corresponding distortion in the energy spectrum as seen by the pixel. This distortion limits the potential energy resolution of the system.
1.2 Imaging detectors technologies

This section provides an overview of different imaging detectors technologies. Characteristics and physical properties of analog film-based system and of a selection of pixel detectors used for X-ray digital imaging will be considered. This should help in better understanding the potential advantages related to hybrid photon counting chip system such as the Medipix2 one described in Chapter 2.

1.2.1 Film-based detectors

The film detector has been the first x-ray detector since 1895 when x-rays were discovered by Roentgen. Although the digital technology is affecting all aspects of medical imaging, film is still today one of most used receptor in clinical application. Understanding its physical properties is important to realize its features and limits with respect to digital receptors. This is why film-based receptors will be described in some detail in this paragraph.

Direct-exposure film consists of a polyester or acetate sheet (“film base”) where a photographic emulsion made of tiny (~1 μm) silver halide crystals (“grains”) is deposited either on one side (“single-emulsion” film) or on each side (“double-emulsion” film) of the base. The most common silver halides are silver bromide (AgBr), silver iodide (AgI) or silver chloride (AgCl).

When radiation of appropriate wavelenght (~0.1÷500 nm) strikes the silver halide crystals, a series of reactions begins that “sensitize” the grain producing a small amount of free silver in the grain

\[ \text{Ag Br}^- + h \rightarrow \text{Ag} + \text{Br}^- \]

The silver atom can then recombine with the free electron to produce a silver atom. The free silver produced in the exposed/sensitized silver halide grains constitutes what is referred as the “latent image”.

---

1 At least four silver atom are needed to sensitize a grain.

2 It is basically a redox reaction where the bromine ion is oxidized and the silver one is reduced.
During the subsequent **development process**, the grains that contain silver nuclei are reduced much faster than those that do not. The greater the number of silver nuclei on a grain (i.e., the greater the exposure of that grain), the faster the developer will reduce the remaining silver to metallic silver. Thus, the grains that had more light hit them will be reduced more quickly and will have a more intense colour (black) from the silver formed.

The film developing process is in fact very complicated, depending on temperature, concentration of developer and pH of chemical solutions.

It consists on four main processes summarized as follows:

1. **“development”**: The developer agent (usually *hydroquinone* $C_6H_4O_2$) reduces the sensitized silver halide grains in metallic silver;
2. **“fixing”**: The fixing solution (usually *sodium thiosulfate* $Na_2S_2O_3$) stops the reduction process when the darkening reaches the right level and removes the unexposed and undeveloped silver halide;
3. **“washing”**: The film is washed on water to remove the fixer and developer solutions;
4. **“dry”**: The film is dried with a hot air flow.
In clinical practice, automated equipments can accomplish all these steps in time varying between 30 to 200 second.

The film blackening is quantified in terms of “optical density” $D$ which is defined by the relation $D = \log_{10} \frac{I_0}{I}$, where $I_0$ and $I$ are the intensities of a light beam before and after passage through the film. Curves which relate optical density to the logarithm of exposure are known as “characteristic” or “H&D” curves (in honour of Hurter F. and Driffield V.C. who were the first to describe them in 1890).

![Image](image_url)

**Fig. 0.3.** Typical characteristic curves of x-ray film receptors. “High speed” film with CaWO screen (a), “no screen” (b) and “high speed” without screen are considered (from [Joh83]).

A typical film characteristic curve (fig. 1.3) shows a central portion where the relationship between optical density and the logarithm of exposure (dose) is roughly linear. For exposure values higher than the latitude interval, the characteristic curve present a flat portion named “shoulder” where the response of the film is poor due to the fact that most of the grains are already sensitized. At low exposure level, the characteristic curve shows another flat portion named “toe”. It is a consequence of the low absorption efficiency of the film receptor so that more there is a minimum photon flux above which the grains are sensitised (this is true especially for barely
film receptor). Finally, an optical density offset is always present due to the intrinsic density of the film base plus the background noise or “fog” (referred as “base plus fog” level). The slope of this straight portion is referred to as “gamma” ($\gamma$) of the film while the range of correct exposure is called “latitude”. The film contrast is related to the latitude and gamma; high-contrast will have a high gamma factor and a narrow latitude and vice versa. The exposure should be chosen to make all parts of the radiograph lie on the straight-line portion of the characteristic curve, ensuring the same contrast for all densities. Over- or underexposure will result in loss of contrast and possibly in the loss of useful diagnostic information [Dan98].

The one of the main limits of the film receptor is its poor x-ray absorption efficiency (only about few percent). Due to its low speed values, film is usually coupled with a fluorescent screen to give the so called “screen-film” receptor. X-ray photons are absorbed by the screen and some of its energy is re-emitted in the form of light fluorescent photons by the phosphor contained within the screen. The light fluorescent photons impinge the film emulsion of the film put in close contact with the screen. After exposure, the film is developed and viewed in the usual way. Typical intensifying screens are made of terbium-activated rare-earth oxysulfide such as gadolinium oxysulphide ($\text{Gd}_2\text{O}_2\text{S}_2$) or calcium tungstate ($\text{CaWO}_4$).

Screen-film is about 100 time more sensitive than simple film (i.e. is faster than film) but does not preserve the same inherent resolution of film. The spatial resolution of the film is mainly limited by the range of secondary particles produced within it. A 50 keV photoelectron have 70 $\mu$m range in the emulsion while the mean free path of silver characteristic x-ray is 400 $\mu$m. The lateral spread is limited by the thickness of the emulsion (~20 $\mu$m). This is why film receptor have excellent intrinsic resolution properties [Dan98]. Instead the resolution of film-screen receptor is mainly limited by the lateral spread of fluorescent photons as they pass from screen to film. This spread can increase if a good contact between film and screen is not properly achieved.

Due to its higher speed, screen-film are usually preferred to direct-exposure films in many clinical applications. Film without screen are used when speed is not a great
deal, as in the radiography of body extremities (like hands and teeth) or whenever extreme detail is required and dose is not a concern.

1.2.2 Phosphor Imagers detectors

CR is based on “image plates” accumulate photon-generated electrons in metastable trapping levels (named “color centers”) when exposed to X-rays. Suitable phosphors are commonly found in the barium fluorohalide family, with BaFBr:Eu$^{2+}$ being a typical example. These charges can be read out in a dedicated system by scanning the plate with a laser which stimulates an optical transition of the trapped electrons. The intensity of this stimulated emission is proportional to the number of the X-ray photons which were absorbed and thus carries the image information.

CR or Storage Phosphor technology represents the natural pathway from analog films to digital radiography [2]. A CR imaging system consists of two elements: the image plate (IP) which records and stores the image information and the scanner unit which reads the plate and digitalize the image data. IPs, also known as Photo-Stimulable Phosphor (PSP) plates, are image sensors in which bunches of microcrystals (about 5 µm in size) of barium fluorohalide doped with europium (e.g. BaFX:Eu$^{2+}$, where usually X=Br, I, Cl) are uniformly coated on a polyester flexible support layer. When IPs are exposed to x-ray photons or radioisotopes such as $^{32}$P, $^{33}$P, $^{35}$S, and $^{14}$C, electrons are released and trapped into metastable energy sites (named “color centers”) induced by the europium ions into the phosphor lattice. This process constitutes the so called “latent image”. Trapped electrons relax back to their ground state naturally or compulsorily when illuminated by red light ($\lambda \approx 550$ nm). The first process is called “fading” while the second one is know as photo-stimulated luminescence (PSL). In both cases luminescence photons ($\lambda \approx 390$ nm for BaFX:Eu$^{2+}$) are emitted from the IP surface.

The scanner unit reads out the latent image by raster scanning the IP surface with a focused laser beam. The intensity of this stimulated emission is proportional to the number of the X-ray photons which were absorbed and thus carries the image information. The PSL light is collected and converted to an electrical signal by a
photomultiplier and finally digitalized by an ADC to form the image. After reading, IPs are exposed to an intense white light to erase the residual information and then can be reused thousands of times if cared for properly.

IPs structure is quite similar to the film screen one and provides the same standard field coverage area (typical imaging fields are 35 cm x 40 cm in chest radiography, and 18 cm x 24 cm and 24 cm x 30 cm in mammography) so CR exploits the same radiographic cassettes as film-based systems with the only difference that the film is replaced by a phosphor plate. With respect to screen-film systems CR offers higher sensitivity (up to 100 times), wider and linear exposure range. On the contrary, the spatial resolution is a bit lower than screen-film. It is limited by the spreading of the fluorescent light beam as well as by and () as well as of the released stimulated light (which is a function of the grain size and thickness of the phosphor material) and depends also on the resolution of the read-out scanner (which depends on the spot size and the laser power).

Due to the lower X-ray conversion efficiency, survey’s doses tend to be slightly higher than for screen-film systems, but the broad and linear dynamic range of storage phosphors helps to avoid faulty exposure and repeated radiographs. IPs are reusable and images are available faster than with film-screen systems and moreover in a digital format so they can be easily processed and archived.

The major drawback of a CR system compared to a film-based system is the start-up cost. Compared to other, fully digital systems, the main disadvantage is the laborious scanning of the plates, which makes real-time imaging impossible.

Due to their properties storage phosphors are suitable for emergency and mobile radiography but they are widely used also in biology (auto-radiography) and physics (dosimetry) fields as charge particle (alpha, beta) and neutrons detectors.

### 1.2.3 CCD-based detectors

A charge coupled device (CCD) imager consists of a series of small metal-oxide semiconductors (MOS) capacitors (i.e. the CCD pixels) organized in parallel columns. Gate electrodes are built on top of an insulating oxide layer and when biased create a depleted zone (“potential wells”) in the semiconductor underneath the oxide. The
photons which penetrate in the semiconductor substrate produce electron-hole pairs which are separated through an applied electric field. The photo-charge generated in the semiconductor from several events accumulates in the potential wells closest to the interaction point.

Different readout architectures exist. The simpler one (“serial readout” scheme) is accomplished by clocking the gate potentials in such a way that the accumulated charge packets are shifted down the pixel columns. In this way subsequent rows are transferred to a readout shift register put on the bottom edge of the matrix. The charge packets of one pixel row are then shifted to the analog output node where are measured by an on-chip charge-sensitive preamplifier and subsequently digitised by an analog-to-digital converter. The output of a CCD results in a serial train of pulses which is well adapted for display on a video monitor.

Fig. 0.4. Serial readout CCD architecture (left). Pixel are defined by the crossing of implanted stop channels and the electrode rows. On the right figure, the charge shifting scheme is depicted.

Alternatively, in order to increase the readout time, “interline” or “frame-transfer” CCDs may be used. Interline transfer CCDs have a photoinsensitive shift register next to each column. The image to be read out is very rapidly (≈ μs) transferred to the adjacent shift registers and the photopixels are then free to continue image accumulation while the shift registers are being clocked out. Interline transfer CCDs typically have less than unity fill factors due to the area taken up by the shift
registers. In **frame-transfer** CCDs half of the length of the columns are covered and can be clocked independently of the uncovered half. These CCDs take advantage of the fact that the columns can be clocked down very quickly (microseconds) without compromising performance, i.e., the bottleneck starts at the preamp. So the image accumulated in the uncovered half of the columns is very rapidly clocked into the covered half, i.e., the frame is transferred. Then the transferred frame is slowly read out while the uncovered half integrates the next exposure. Although the uncovered half has 100% fill factor, the CCD must be twice as large to accommodate the storage frame.

![Fig. 0.5. Structure of “frame-transfer” (left) and “interline-transfer” (right) CCDs.](image)

CCDs are directly responsive to x rays, as well as to light but their use as direct conversion x-ray detectors is limited both by stopping power (the depletion regions of most commercially available CCDs are only a few microns thick) and radiation damage concerns. In medical X-ray imaging the x-ray conversion takes place in phosphor screens (like CsI(Tl) or Gd₂O₂S) to increase the photon absorption efficiency. But as already mentioned, the indirect detection scheme limits the achievable spatial resolution by the light spreading of the scintillator layer.

Because the size of CCDs is limited, it is necessary to employ some means of demagnification between screen and CCD. This can be achieved either by optical lens
coupling or by using a fibre optic taper. Fibre optic taper is preferred due to smaller light losses [Yaf97].

**Fig. 0.6.** Side view of a standard (right) and of p-n type (left) CCD. The former CCD has to be associated to a scintillator to detect x-ray while in the latter one direct absorption is performed by irradiating the CCD backside (from [Pon05]).

CCDs have an high intrinsic spatial resolution due to their high spatial sampling pitch. CCDs with pixel sizes as small as 10 µm are available, but the final spatial resolution is deteriorated mainly by the lateral spread of the light photons produced in the phosphor screen. CCD systems for medical applications may be as small as 25 µm, but the spatial resolution is in the order of ~5 lp/mm [Eva02]. The dynamic range of CCDs is determined by the depth of the potential wells minus the integrated noise (charges due to thermal noise). With low noise a dynamic range of about 10^5 can be achieved [Far95]. Although pixels can be clocked out of CCDs at rates of tens of MHz, the noise rises with the readout rate. Cooling the CCD is generally needed to reduce the dark current of thermally generated electron-hole pairs. For most CCDs, optimum noise performance occurs for cooled, slow-scan rates below 50–500 kHz, depending on the CCD and the analog to digital conversion electronics. At slow-scan rates, modern scientific CCDs readily achieve noise figures of 10 electrons rms/pixel. Read-out times are in the order of a few seconds [Far00].

Fill factor refers to the fraction of the imaging area of the CCD that is photoactive. Serially readout CCDs with 100% fill factor are most commonly used for x-ray detector work. These CCDs have the disadvantage that the imaging structure is also the readout structure, so image signal which arrives while the CCD is being read out winds up smeared over the shifting image already accumulated. Thus, it is usually necessary to stop the x-ray signal during read out, thereby imposing a duty cycle.
1.2.4 Flat-panel detectors

Flat-panel imaging device technology is strictly related to that of flat-screen displays used for laptop computers, PC monitors and televisions. Such devices are fabricated using thin layer of amorphous silicon (a-Si) where large active matrix (AM) of pixel can be manufactured via standard photo-lithography and chemical etching techniques. Each pixel usually house specific components like photo-diodes, storage capacitors, diode or transistor switch depending on the specific design. Amorphous silicon allows to overcome the size limit of the crystalline silicon and have the further advantage of being radiation-hard.

The readout switches connect a row of pixels to charge amplifiers located at the bottom of the columns. The electric charge pattern stored in the pixel capacitors is sensed by an electronic readout mechanism and an analog-to-digital conversion process produces the digital image (direct conversion). In this way the readout time can be significantly improved with respect to CCD systems.

The two designs of flat-panel detectors (FPD) which have so far been most widely used in clinical service are known as “indirect-conversion” and “direct-conversion” FDP detectors [Cow08].

Indirect-conversion FDP detectors are currently the most successful one. Their architecture is based on a combination of a layer of x-ray fluorescent material with a a-Si:H AM readout array. First prototype devices used Gd$_2$O$_2$:Tb intensifying screen as photon converter layer while modern one use a layer of thallium-activated caesium iodide (CsI:Tl). Such a material is an excellent x-ray absorber and have a channelled (“needle-like”) crystal structure which minimize the scatter of fluorescent light. The needle crystal are typically 5 – 20 μm in diameter while the scintillator layer is about 500-600 μm thick.

The indirect-conversion AM consists of amorphous hydrogenated silicon (a-Si:H) photodiodes. The light striking each photodiode generates a charge which is integrated in the pixel capacitor (fig. 1.10(a,c)). Being low-noise devices, the photodiodes provide a very large dynamic range, of the order of 40 000.
The photo-charge signal is read out by activation of scanning control lines for each row of the device, connected to the gates of TFTs located on each detector pixel. An entire row of the detector array is activated simultaneously and the signal is read on lines for each column in the array which connects all the TFT sources in that column to a low-noise charge amplifier. The amplified signals from the columns are then multiplexed and digitized.

![Diagram of an indirect-conversion FP device](image.png)

**Fig. 0.7 - Schematic drawing of an indirect-conversion FP device (Trixell Pixium device).**

Commercial available indirect-conversions FDPs offer acquisition area up to 43 cm x 43 cm, with a pixel size of ~ 140 μm a readout time of ~ 1ms (e.g. Pixel Pixium 4600).

On **direct-conversion** FPD detector a layer of amorphous selenium (a-Se) is used as x-ray photo-conductor material to absorb the incident x-ray photons. The a-Se layer is deposited on a a-Si:H AM array which comprises a regular matrix of storage capacitors and thin-film transistor (TFT) switches. During image acquisition, x-ray photons directly induce free electrical charge carriers in the a-Se layer, but with no emission of fluorescent light [Cow08]. An high bias voltage of about 10 V/μm (i.e. 5 kV for a 500 μm thick layer) is required to separate and collect the induced charge carriers. In such a way the lateral spreading of charge is negligible and the loss of
spatial resolution is very low. This feature allows to increase the thickness of the a-Se layer preserving a good spatial resolution.

The image charge is then collected by the pixel electrode and accumulated onto the pixel storage capacitor. The pixel electrode and storage capacitor are connected to the TFT switch of each pixel. The readout device can be similar to that used with amorphous silicon (fig. 1.10(b,d)). The external scanning control circuit generates pulses to turn on all the TFT switches on a row of the array and transfers charge from the pixel capacitors to the readout rails (columns). The charge is then collected and amplified by an amplifier on each rail and the data for the entire row are multiplexed out. This sequence is repeated for each row of the array. The readout can be in real-time thus this approach has the potential to be used both in radiography and fluoroscopy [Yaf97].

The a-Se photon absorption efficiency in the energy range of radiography is lower than the that of CsI:Tl, so that an a-Se layer 500 μm thick is typically used.

---

**Fig. 0.8. Schematic cross-section of a direct-conversion FPD**

Between each acquisition the device must be reconditioned illuminating the detector surface with light to flush away electrons trapped at the dielectric/a-Se interface used to separate the top bias electrode to the a-Se layer (fig 1.9). This process takes few tens of seconds before to start a new acquisition.
Fig. 0.9. Comparison between indirect detection FPDs (left column) and direct detection FPDs (right column). Fig. a) and b) shows a schematic side view of incident radiation interacting with an array pixel. Fig. c) and d) draft the equivalent circuit of an array pixel along with gate driver and preamplifier electronics. Finally, fig. e) and f) are microphotographs of 97 mm pitch and 100 mm pitch pixels for indirect detection and direct detection, respectively (pictures are from [Ant00]).

FPDs sensing areas as large as about 35 cm x 45 cm, with a pixel pitch of ~ 100 μm, are available so that FDP can be used for full-field radiography applications.

The necessity to implement the photodiode leads to a reduced fill factor, i.e. a reduction in sensitive area per pixel cell. The main advantage of AMFPI over CCDs is that large areas can be covered. The biggest drawback is the high electronic noise of ~700 e- [ZHA05] per pixel even with pixel amplification, without pixel amplification is a factor 2-4 higher, which makes this technology not suitable for low X-ray energy detection.
1.2.5 CMOS detectors

The further step on the evolution of digital imaging devices are the CMOS devices where the commercial CMOS technology is exploited to design digital circuitry at pixel level ("active pixel" devices).

The two main types of CMOS sensors are the "passive pixel sensor" (PPS) and the "active pixel sensor" (APS). In the former, a photodiode is integrated in a pixel together with selection switches, which connect the photodiode directly to the output line for readout. In the latter, an amplifier integrated in each pixel directly buffers the charge signal. Today most CMOS imagers have an APS structure because of its better performances [Tur01]. CMOS sensors are designed as monolithic or hybrid devices.

The Monolithic Active Pixel Sensor (MAPS) device are made in a CMOS technology, are used today as an alternative to CCDs for many applications in visible light imaging. Such a device integrates on the same chip the sensor and the first amplification circuit.

The advantages are in particular low cost since they are produced in a standard process and the possibility of random access to each pixel. The use of this technology for the detection of charged particles is challenging since only the very thin epitaxial layer of the silicon is available as sensitive volume.

This devices can be fabricated using the commercial CMOS VLSI technology [Tur01] or other non-standard technologies like DEPFET (depletion field effect transistor) or SOI (Silicon on insulator).

Fig. 0.10. Example of a monolithic active pixel sensor showing a field effect transistor realized on a high-resistivity silicon substrate (from [Pon05]).
In hybrid devices the detector is made of a pixellated single crystalline sensor which is bump bonded to a custom VLSI readout chip (the sensor is segmented with the same geometry as the readout chip). The radiation sensor element and the readout can be processed separately allowing for independent optimisation of readout and sensor. Different sensor materials can be used with the same readout chip.

CMOS detector sizes are usually limited to few square centimetre due to the practical size of a CMOS chip. Even if these chips are produced in a process using 200mm (or even 300 mm) diameter, low-resistivity silicon wafers with an epitaxially deposited high-resistivity layer, with standard technology the maximum chip size achievable is limited to about 25 mm x 25 mm, due to the reticule size of the wafer stepper. Alternative techniques to circumvent this limitation exist but they are non-standard, expensive, and, moreover, the yield of the manufacturing process is inversely proportional to the chip area [For02].

The strategy to achieve large sensitive areas is that of tiling together multiple electronics chips, all of which are then bump-bonded to the same large semiconductor sensor. Dead area between neighbouring chips is avoided because the electronic cells at the chip boundary are connected to larger sensor diodes (fig. 1.12). Such multi-chip hybrids, also called ladders, can then be tiled into an even larger sensitive area, although in such cases dead regions become unavoidable [For02].

![Fig. 0.11. Left: schematic view of a multi-chip module with large pixel at the inter-chip region (from [Loc04]). Right: Picture of a CdTe sensor for an hybrid multi-chip ladder (XPAD module). Inter chip region has larger area pixel to avoid dead areas between neighbouring chips (from [Bas08]).](image-url)
1.2.6 Single photon counting hybrid detectors

Single photon counting with hybrid pixel detectors has been introduced as a suitable method for direct digital imaging [Fis98] - [Cam98]. The hybrid architecture with a sensor bump bonded onto the read-out electronics has the advantage that both electronics and sensor can be optimized independently and a sensor material optimal for the specific application can be chosen.

Due to these such a promising characteristics, several imaging detectors projects use the direct detection photon counting hybrid pixel system approach for many different imaging applications. One of them is the Medipix project which will be illustrated below in § 1.2.7. A selected list of other active projects follows.

- **MPEC (Multi Picture Element Counter)** is the name of the photon counting x-ray project at Bonn University [MPEC]. The chip design has undergone several iterations [Lin01]. The first prototype version was developed in 1997. It has been done in the AMS 0.8 µm technology. **MPEC 1.0** consists of 756 pixels divided into 12 columns and 63 rows. The pixel size is 433.4 µm × 50 µm size in order to be able to use already existing silicon pixel sensors [Fis98].

  The second generation (**MPEC 2.x**) has been done in the 0.8 mm AMS CMOS process with two metal layers and has square pixels instead of the rectangular ones of the first series. The current version (**MPEC 2.3**) features an active area of 6.4 mm × 6.4 mm is structured into 32 × 32 pixels of 200 µm × 200 µm size. Every pixel cell contains a preamplifier, two independent discriminators, and two 18 bit counters (fig. 1.13).
A coarse discriminator threshold is set globally, and a fine adjustment can be applied dynamically for both discriminators in each pixel. This dynamic adjustment is performed by storing a correction voltage on a capacitor. The independent discriminators allow an energy window to be set, which can be an array of 32 x 32 pixels at a pitch of 200 \( \mu m \times 200 \mu m \). Each pixel contains a pair of discriminators, two 18-bit counter cells and a dedicated window logic which allows the counters to record only photons within a definable energy region, a feature used for contrast improvements. The chip was tested with a wide range of sensor materials such as Si and GaAs [21].

Multichip modules (MCM) have been built by four chips arranged in a 2 x 2 array which leads to a 64 x 64 sensor pixel geometry. The four MPEC 2.3 chips are bump bonded to 1.3 cm x 1.3 cm CdTe or Si semiconductor pixel sensors [Loc04]. It was also the first photon counting pixel detector system featuring CdTe sensors and multichip modules.

- In the behalf of the PILATUS (pixel apparatus for the SLS) project, located at the Swiss Light Source (SLS) of PSI\(^3\) (Villigen, CH), a large-area detector for X-ray crystallography has been built. PILATUS detectors are two-dimensional hybrid pixel array detectors, which operate in single-photon counting mode. Data are readout in continuous mode in of 5 ms.

---

\(^3\) Paul Scherrer Institute
Several versions of the PILATUS chip have been designed till now [www02]. The first generation PILATUS chip was designed in 2000. Each chip contains an array of 44 x 78 pixels with a pixel size of 217 μm. The active area spans 10 x 17 mm². Each pixel contains a charge-sensitive preamplifier and shaper, a single-level comparator with a 4-bit individual threshold adjustment, a 15-bit counter with a clock frequency of 10 kHz. A PILATUS module consisting of a single silicon sensor bump-bonded to an array of 8 x 2 chips was realized. The sensor is a continuous array of 366 x 157 pixels without dead areas. Double-sized pixels are used at the chip boundaries to span the gap between neighbouring chips. The 16 chips of a module are read out in parallel at a clock frequency of 10 MHz, which leads to a read out time of 6.7 ms for one module.

![Image](image.jpg)

Fig. 0.13. The first generation PILATUS module obtained by tiling 8 x 2 chips.

The latest ASIC PILATUS-II chip was designed in a commercial CMOS 0.25 μm technology (2004). It is arranged as a matrix of 60 columns and 97 rows of square pixels measuring 172 μm on the side. The threshold can be tuned with 6 bits and the pixel counters have a depth of 20 bits with a maximum count rate ~1.5 MHz/pixel/s. The PILATUS-II modules consists of a Hamamatsu sensor bump-
bonded to an array of 8 x 2 chips using indium balls. The 16 chips of a module are read out in parallel within a read-out time of ~2 ms. The “PILATUS 100K” detector consists of a single module and has 487 x 195 pixels. The active area covers over 8.4 cm x 3.4 cm. Such a detector is in use at the X04SA materials science beam line at the SLS for surface diffraction experiments since 2006. The “PILATUS 6M” (fig 1.13) is designed for protein crystallography studies and consists of 5 x 12 modules with 2463 x 2527 pixels and a total active area of 424 cm x 435 cm. The “PILATUS 2M”, composed of 3 x 7 modules with 1475 x 1467 pixels and a total active area of 25.4 cm x 25.2 cm, is designed for coherent small angle scattering experiments.

Fig. 0.14. The PILATUS 6M (left) and 2M (right) detectors (from [www02]).

- The XPAD (X-Ray Pixel with Adaptable Dynamics) is a photon counting hybrid chip developed at ESRF4 (Grenoble, FR) for material science investigations (SAXS5 and X-ray diffraction) with synchrotron light source [www3]. The project started in 1999, with a 1st prototype XPAD1 tested in 2000-2001 and followed by a 2nd version XPAD2 (2002-2003). The 3rd generation XPAD3 has been processed and is currently under test. XPAD3 extends its applications range also to medical field [Pan07].

  The prototype chip XPAD1 was processed using the 0.8 mm CMOS technology by AMS [Bou03]. Each chip contains 24x25 pixels. Each pixel shapes the signal,

---
4 European Synchrotron Radiation Facility
5 Small angle x-ray scattering.
discriminates and stores counts in a local 16 bits counter. Overflows are read
during exposure and stored in a common logical unit to reach a total dynamical
range of 32 bits per pixel. The detector can operate between 10 and 24 keV with
an estimated energy resolution of 1.5 keV and count rates between 0.01
photons/s/pixel to $2.5 \times 10^6$ photons/s/pixel. For acquisition and read-out
purposes, the prototype chips [11,12] were mounted on an epoxy card together
with a few logical elements and an ALTERA programmable logic device. The
PLD was also used as a memory for the external counters. The whole system
was then monitored with a PC for the test data collection.

The XPAD2 electronic chip is designed in AMS 0.8 µm technology with 600
pixels of $330 \times 330$ µm². Each pixel includes a charge amplifier, a discriminator
and a 15 bits counter. The discriminator thresholds are set for the whole chip
and a fine adjustment (6 bits) is allowed for each pixel. A calibration charge can
be injected in the charge amplifier via a small capacitor. Bump-bonded on
silicon sensor its maximum random rate amounts to about $10^6$ photon/s per
pixel. Data can be read out during exposure time by scanning the pixel counters
(15 bits) overflow at a rate higher than the counter filling and adding it an
external 16 bits counter. Thus, a dynamic range of $10^9$ can be achieved. At the
end of the data acquisition, a fast readout system based on a Altera’s “Nios”
board allows for reading the full detector in less than 2 ms. The system includes
enough local memories to store either 423 frames with 15 bits per pixel or 210
frames with 31 bits per pixel. Finally, all data are transferred on the acquisition
PC using a 100 MB ethernet link.
A large area module has been developed holding 8 \texttt{XPAD2} chips of 16 mm x 8 mm active area bonded to one 16 mm x 64 mm Si sensor. Eight of these modules are then arranged on a staggered ceramic support to obtain a ~ 25 cm x 25 cm large-area detector named PIXSCAN (fig. 1.13) aimed to small-animal imaging [1].

The last \texttt{XPAD3} chip [Pan07] was designed in IBM 0.25 µm CMOS technology to achieve a square pixel measuring 130 µm on the side with 9600 pixels (80 x 120). The pixel cell (fig. 1.12) is composed of a charge sensitive preamplifier, an operational trans-conductance amplifier followed by a set of current comparators for energy selection. The selected pulses feed a 12 bits counter associated with an overflow mechanism. Nine configuration bits are available in each pixel for control. The \texttt{XPAD2} features have been improved to provide high-counting rate over 109 ph/pixel/mm$^2$, high-dynamic range over 60 keV, very low-noise detection level of 100e$^-$ rms, energy window selection and fast image readout less than 2 ms/frame.

Readout of the chip is performed a 4 bit wide LVDS bus during exposure. Many \texttt{XPAD3} circuits can be assembled in arrays to get a full usable picture. All of them can be read in parallel resulting in a 2 ms picture read-out time.
Fig. 0.16. Schematic view of the XPAD3 pixel cell (from [Pan07]).

Two different chips have been designed with different analog front-ends. The XPAD3-S [Pan08] is dedicated to crystallography while the XPAD3-C [Bas08] is for medical imaging applications. The “S” (as in silicon) version is for hole collection at and offers an energy range of 35 keV with a single threshold for energy selection. The “C” version (as in CdTe) accepts electrons and has an energy range of 60 keV with a windowed energy selection obtained with two thresholds.

- **DIXI** (Digital X-ray Imaging) is a readout chip for a hybrid pixel detector developed at Uppsala University aimed for use in dynamic medical X-ray imaging [Edl04]. The main features of DIXI are a photon counting capability and the implementation of two counters in every pixel cell. The current version has the size of ~1 cm² with 31 x 32 pixels, each with a size of 270 x 270 μm². The chip has been fabricated in a 0.8 μm N-well CMOS process with two metal layers. The chip has been designed with very little dead space at the edges, thus allowing several chips to be assembled on a single sensor.
The pixel cell (fig. 1.12) consists of a charge sensitive preamplifier followed by a shaper and the output is a semi-Gaussian shaped pulse. A high-pass filter is placed before the discriminator to decouple it from DC voltage shifts in the front-end. The discriminator is constructed by using time-over-threshold technique. An externally adjustable threshold is set globally for the chip. An output signal is obtained only if the pulse height exceeds the threshold level and the time the pulse spends above the threshold determines the width of the differential output signal from the discriminator. The amplification in the discriminator is made large and a clamping circuit is implemented in front of the counter to limit the swing of the differential signal. The aim is that the width of the output pulse should have a small dependence on the time-over-threshold. The counters are implemented as capacitors which are uncharged before the start of an image acquisition. Every time the differential output from the discriminator signals a hit a small amount of charge is drained from the capacitor. When the image acquisition is complete the voltage level across the capacitor is read out synchronously for all pixels at 1 MHz and it is digitised in the control system by a 16-bit resolution analogue-to-digital converter (ADC). The two counters are read out in parallel. The dynamic range of each counter is 12 bits. The design with two counters makes it possible to acquire two images separated in time by 1 ms before both images are read out. The threshold level
of the discriminator can be changed from the first to the second image to make the chip sensitive to different parts of the X-ray spectrum. The front-end is sensitive to both electron and hole collection.

1.2.7 The Medipix project

The Medipix project [www1] started in the second half of ‘90s from the collaboration agreement between CERN, University of Freiburg (Germany), Glasgow (Scotland), Universities and INFN of Naples and Pisa (Italy). The aim of the Medipix collaboration was to realize a new detector for X-ray radiography based on the hybrid architecture, direct photon detection and the single photon counting concepts. All these properties was very promising for X-rays medical imaging applications.

- Starting from the early 1990’s, the CERN microelectronics group started to develop of a new type of vertex detector for the Large Hadron Collider (LHC) experiment. At that time, in the framework of the RD19 project, the Omega chip series was designed. In particular, the Omega3/LHC1 chip, bonded to 200 \( \mu \)m Semi-Insulating GaAs sensor, was promising for X-ray imaging application [DaV97]. The Medipix readout chip is currently in its third generation. A prototype of the Medipix3 chip with a 8 x 8 pixel matrix and a pitch of 55 \( \mu \)m x 55 \( \mu \)m has been produced and tested [Bal06].
1.2.7.1 The Photon Counting Chip (Medipix1)

Thanks to the large experience of CERN in hybrid pixel detector design for high energy physics (HEP) experiments, the first detector developed in the framework of the Medipix collaboration was delivered in 1997 [Cam98]. It was designed in SACMOS1 (1 µm Self-Aligned Contact CMOS) technology with 2 metal layers and it’s known as Photon Counting Chip (PCC) or Medipix1. The pixel matrix contains 64 x 64 (4096) square cells, 170 micron side. Each cell houses a Charge Sensitive Amplifier (CSA) followed by a 3-bit adjustable comparator (for the fine tuning of the energy threshold within the matrix) and a 15-bit pseudo-random counter capable to store up to 32767 single events. The detector is sensitive to positive charge with a minimum threshold of ~1500 e (corresponding to ~5.5 keV charge deposition in a Si sensor) and maximum count-rate of ~2 MHz.

The PCC measures 1,225 cm x 1,4 cm yielding a total area of ~1,7 cm$^2$ and sensitive area of ~ 1,2 cm$^2$. A 16-bit bi-directional bus is used for configuration as well as for data readout. The maximum readout frequency allowed is 10 MHz so one complete data frame can be read in 384 µs.

The chip has been bonded to 300 µm Si and 200 µm GaAs sensors.

![Fig. 0.19. Schematic of the Medipix1 pixel cell.](image)

Two read-out systems were developed for Medipix1 control and data acquisition. The Medipix1 Readout System (MRS), designed by Laben S.p.A., Milano (Italy) together with the INFN of Pisa, was a VME-based system [Ame99]. It was a rather
complex system composed of a PCI bus to VME bus interface, a VME crate and a custom VME board, a few power supplies and a pulse generator. Later, the Nikhef group designed a new and simpler read-out board, called Medipix1 re-Usable Read-Out System (MUROS1), which interfaced a standard PC by two commercial PCI cards (by Nuclear Instruments) and the Medipix1 chip-board [Bar00]. The Naples group provided the Medisoft 3 software to full control the Muros1 readout system. It was written in C-code under LabWindows which provides a windows-based environment.

![Fig. 0.20. Pictures of the Medipix1 chipboard (left) and MUROS readout board (from [Gie05]).](image)

A third simple and cheap read-out system named portable MUROS1 (pMUROS) was developed by the Naples group for auto-radiography applications [Mai02].
Fig. 0.21. Picture of the pMUROS board developed by the Naples group [Mai02].
1.3 Summary

In this chapter a selection on analog and digital imaging devices has been overviewed trying to underline their main physical and design properties.

In spite of its inherent limitations due to a lack of exposure latitude film based systems still represent the big fraction on the market of medical X-ray imaging systems because its functional utility and perceived high-imaging quality.

In fact, film/screen receptors have an inherent high spatial resolution typical of analog receptors whilst in digital detectors the spatial resolution is by the pixel dimensions $d$. Even if in general terms the spatial resolution analog film is always higher than the digital detectors one. Nevertheless, further experience has suggested that a high value of limiting resolution is not as important as the ability to provide excellent image contrast over a wide latitude of x-ray exposures for all spatial frequencies up to a more modest limiting resolution [Yaf97]. In digital system, the ability to detect low-contrast details depends on the contrast and signal-to-noise ratio properties more than on resolution properties [Gam03]. Modern digital radiographic system can thus provide high resolution images, as well as allowing the implementation of computer image processing techniques, digital archiving and transmission of images and extraction of medically useful quantitative information from the images.

The trait d’union between analog and digital concepts is the Computed Radiography technology which is very similar to screen-film systems but offers many advantage of digital concept. CR systems exploit an analog receptor (image plate) to acquire and store the image data but are able to record images digital form.

The last decade has seen rapid development and clinical adoption of active-matrix flat-panel (FP) imagers for diagnostic x-ray imaging [Zha]. FP detectors are mature technologies that have been rapidly gaining in clinical acceptance. Two different architectures are available based on indirect and direct conversion concepts. FP detectors manufacturers seem to favour the indirect-conversion devices which offers wider clinical applications even if direct-conversion detectors still have an important
role in full-filed digital mammography. FP s provide better image quality than traditional screen films and computed radiography but further improvement is desirable, especially in spatial resolution and low-dose performance [Mon05].
Imagers based on charge coupled devices (CCDs) have obtained a steadily increasing importance in imaging applications where they replace film as the image receptor due to the advantages a digital system implies. Usually CCD cameras are used to digitise the output of x-ray image intensifier (XRII). Their development could profit from the technology push from the camcorder market. CCDs is an intrinsically high resolution device due to the small pixel size (~10 μm) but when coupled to optical taper and scintillating layer degrades they spatial accuracy. Their readout frequency is usually kept low to reduce the inducted noisy. High dynamic range is available but requires a cooling system.

Novel detectors are based on CMOS circuitry integrated on the pixels (active matrix). While in a CCD and FP sensors, every pixel’s charge is transferred through a limited number of output nodes (often just one for CCDs) to be converted to voltage and digitized, in CMOS sensors each pixel has its own charge-to-voltage conversion, and the sensor often also includes amplifiers, noise-correction, and digitization circuits, so that the chip directly outputs digital bits. As drawback, these other functions can increase the design complexity and reduce the area available for light capture. With each pixel doing its own conversion, uniformity is lower.

CMOS imagers have the great advantage of exploiting the growing commercial CMOS technology but they offer a small area coverage which limits their use in diagnostic radiology. At present, the size limitation of a CMOS chip is the only important issue of CMOS imagers which has to be solved in the coming years.

CMOS readout chip can be coupled to semiconductor sensor to give direct detection hybrid detectors. The development of hybrid pixel technology had its origin in the demand for high performance vertex detectors for particle physics experiments. Semiconductor converters have significant advantages over phosphors: Semiconductors directly convert the x-ray energy into electrical charge, which often simplifies the design of the detector. Compared to phosphor converters, semiconductors are also usually much more efficient, resulting in more charge carriers, are more linear and less noisy, and the charges are more rapidly and more efficiently collected. The disadvantages of semiconductors that have limited their use as x-ray converters is that large area semiconductor screens are difficult to fabricate,
thick detectors are hard to make, and the semiconductor of choice, namely silicon, has relatively low stopping power [Rev. Sci. Instrum., vol. 73, no. 8, August 2002].

The most advanced detector imaging projects as the Medipix one exploit the photon counting acquisition mode and the direct conversion hybrid design. This work is accomplished in the framework of the Medipix collaboration and is strictly related to the Medipix2 detector, the subject of the next chapter.
1.4 Bibliography


Chapter 1 – X-ray Imaging Devices


[PILA] PILATUS project web site : http://pilatus.web.psi.ch/pilatus.htm


[MPEC] MPEC project web site : http://hep1.physik.uni-bonn.de/MainFolder/documents/article/Research/XRay/MPEC_Project/Index

Chapter 2:

The Medipix2 chip

Abstract - The Medipix2 (MDPX2) is the second generation of a family of single-photon counting readout ASICs\(^6\) developed at CERN in the framework of the Medipix Collaboration [www1]. The Medipix2 consists of 256 x 256 square cells of 55 \(\mu\)m x 55 \(\mu\)m each for a total detection area of 1.98 cm\(^2\). Each cell embeds a differential charge sensitive amplifier, two comparators forming a window discriminator and a 13-bit pseudorandom counter. The counter logic, based on a shift register, also behaves as the input/output register for the pixel. Each cell also has an 8-bit configuration register which allows masking, test-enabling and 3-bit individual threshold adjust for each discriminator. The chip can be configured in serial mode and readout either serially or in parallel.

The design of the Medipix2 and its existing or under development readout systems will be described as comparison with the acquisition system described in Chapter 3.
Picture of a Medipix2 hybrid detector (from [www2]).
2 The Medipix2 chip

Medipix2 (MDPX2) is the second generation of a family of single-photon counting readout ASICs developed at CERN in the framework of the Medipix Collaboration [www1].

The former Medipix1 chip (see Chapter 1) had demonstrated the potential of direct detection photon counting hybrid pixel detectors in x-ray imaging applications. At the same time, Medipix1 had shown several limitations:

- poor spatial resolution due to the side length of the pixel (170 µm);
- the chip was not tilable due to the large dead area around the chip edge (~500 µm);
- the chip could only be accessed through a parallel port (16-bit);
- the chip was able to collect only positive input charges;
- the leakage current compensation was done only at the column level and was found not to be uniform in some detectors;
- the analog bias voltage was externally provided from required a complex setup.

The excellent results and limits showed by the Medipix1 chip both stimulated the design of a new ASIC. The new chip Medipix2 was designed in commercial 0.25 µm CMOS technology which allowed to reduce the pixel size up to 55 x 55 µm² but improving the pixel cell design. The main benefits of such a small pixel were to reduce the input capacitance and to increase the spatial resolution limit.

Two different MDPX2 releases exist: the Medipix2 and the Medipix2MXR2 improved version. Both will be discussed.
2.1 The Medipix2 Photon Counting ASIC

2.1.1 Introduction

Medipix2 is a photon counting ASIC [Llo02] developed at CERN in the framework of the Medipix2 collaboration (see Chapter 1). Combine with different pixellated semiconductor materials (e.g. Si, GaAs, CdTe) it can be used as readout chip for direct conversion hybrid detector.

![Diagram of Medipix2](image)

Fig. 0.22. On the left the Medipix2 passivation openings. On the right the Medipix2 floor plan: the sensitive area with 65536 square pixels of 55 µm² (blue), and the non-sensitive area (green) are shown.

The overall chip dimensions are 16120 x 14111 µm² as shown in fig. 2.1. The sensitive area (14080 x 14111 µm²) consists of a 256 x 256 square pixels of size 55 µm x 55 µm and takes about 87 % (~2 cm²) of the total area. The non-sensitive part (“periphery”) is located at the bottom of the chip in order to minimize the dead area in the other three edges. It houses the bonding pads for the chip connection, the bias DACs and the I/O control logic. Due to presence of the I/O periphery on the bottom side, the Medipix2 chip is buttable only on three sides. It means that 2xN chip arrays are allowed. In order to achieve large sensitive areas, multiple chips are tiled together and the bump bonded to the same semiconductor sensor. Problems related to the
dead area between adjacent pixel are limited using larger sensor diodes [For03]. The
2x2 array ("quad") has been the first multi-chip assembly delivered to the
coordination [Llo04].

The Medipix2 chip uses a serial, high-speed LVDS\textsuperscript{8} logic for setting the
configuration register of the entire pixel matrix and for setting the internal DACs.
Readout can be performed either serially through the same LVDS lines or in parallel
by using a 32-bit parallel, single-ended CMOS readout bus [For03]. The Medipix2
allows for the collection of both electrons and holes.

Medipix2 does not feature continuous readout mode. In fact, image acquisition is
governed by the SHUTTER signal. When this signal is high pixel counters are locked
and their contents can be read (readout operation). When the SHUTTER is low, pixel
counter are active (counting operation) and no readout operation is allowed. It means
that data are available only after that acquisition is stopped. When fast frame
acquisition is required, the maximum frame rate available will be limited both by the
readout frequency and the readout time ("dead time").

The chip is powered by three independent 2.2 V power supply lines: \textit{VDDA} (analog
supply), \textit{VDD} (digital supply), \textit{VDDLVDS} (LVDS drivers supply). The chip static power
consumption is about 550 mW (250 mA at 2.2 V).

The Medipix bare chips are glued and wire bonded to a printed circuit board
(“chipboard”), which serves as a routing layer and as a mechanical support. Electrical
connections between the chip and the carrier board are established with ultrasonic
wire-bonding technique.

\textbf{2.1.2 The Medipix2 pixel cell}

The Medipix2 pixel cell can be divided in two blocks (fig. 2.2): The \textbf{analog part}
which includes the charge sensitive amplifier (CSA) and the window discriminator;
and the \textbf{digital part} formed by the Double Discriminator Logic (DDL), one 13-bit
shift register, one 8- bit Pixel Configuration Register (PCR) plus other auxiliary
CMOS logic for counting and data shifting.

\textsuperscript{8} Low Voltage Differential Signal
When a charged particle or a photon interacts in semiconductor sensor electron and hole pairs are generated and drifted towards the collection electrode by a high electric field (i.e. the sensor bias voltage). The generated charge $Q$ is then integrated onto the feedback capacitor $C_f$ by means of the charge sensitive amplifier (CSA) giving rise, ideally, to a voltage step at the CSA output with an amplitude equal to $Q/C_f$. The output pulse is then compared with two different thresholds that form an energy window discriminator. If the detected charge falls inside this energy window the digital counter is incremented.

### 2.1.2.1 The MDpx2 analog circuitry

The MDpx2 CSA (fig. 2.3) is based on the “Krummenacher scheme” [Kru91]. It integrates and shapes the input charge and compensates for positive or negative input DC leakage currents at pixel basis. The dynamic range of the CSA for both collection modes is ~85 ke$^{-}$ with a nominal gain of 10.5 mV/ke$^{-}$. The output equivalent noise charge (ENC) is about 100 e$^{-}$ rms.
The energy window discriminator is based on two identical branches made of a transconductance amplifier (OTA), a 3-bit threshold adjust and a zero-crossing discriminator circuitry (Zx) whose output is gated with the “mask” bit (fig 2.4).

The voltage signal coming from the CSA stage ($V_{\text{in}}$) is compared with the global high ($V_{\text{TH}}$) and low ($V_{\text{TL}}$) thresholds. The three independent selectable current sources are used to minimize the pixel to pixel threshold variation due to local transistor mismatch and power distribution voltage drops. By properly tuning these 3-bit DAC the pixel to pixel threshold variation can be minimized [Llo03].
2.1.2.2 The MDpx2 digital circuitry

The digital part of the pixel cell (fig. 2.5) is composed of the Double Logic Discriminator circuit (“DDL”), one 13-bit shift register (“SR/C”) and one 8-bit Pixel Configuration Register (“PCR”).

The signal coming from the window discriminator outputs are first compared by the DDL circuitry. The DDL is an asynchronous logic that uses the time-over-threshold pulse (“hit”) from the two discriminator branches to generate an output pulse (CLK_COUNTER).

The DDL can operate in two different modes:

- **SINGLE MODE**: an output pulse is generated when an hit from the low threshold discriminator arrives. The output of the high threshold discriminator is ignored. The *Single mode* is set when the high threshold (THH) level is lower than the low threshold (THL) one.
- **Window Mode**: an output pulse is generated when the low threshold discriminator generates one hit whilst the high threshold discriminator is quiet. The Window mode is set when the high threshold (THH) level is higher than the low threshold (THL) one.

The output pulse width can be set through the 8-bit current global DAC **IDelayN** (i.e. a set of IDelayN = 50 nA (2552 binary DAC set) corresponds to ~300 ns pulse width).

The output of the DDL is the clock signal of the following 13-bit shift register counter (SR/C) which is used for two different roles depending on the status of the shutter control signal (fig. 2.7):

- **When shutter is low** (“counting mode”) the 13-bit SR acts as pseudo-random counter, with the feedback of the 10th and 13th bits [Hor80]. With such configuration the maximum dynamic range is 8001 counts (instead of the expected 8192 of a common 13-bit counter).

- **When shutter is high** (“counting mode”) the SR/C behaves as shift register. The pixel’s SRs within the same column are daisy-chained to form a unique 3328-bit shift register. Such a configuration is used for data readout, after an acquisition phase, or to set the pixel configuration registers.

![Fig. 0.28. Schematic of the SC/R. The p0 bit and clk signal are selected by the shutter signal.](image)

The **Pixel Configuration Register** (PCR) is a 8-bit register which stores the pixel configuration settings, that is:

- **Low-threshold setting** (3 bits) to adjust the low threshold voltage (THL)

- **High-threshold setting** (3 bits) to adjust the high threshold voltage (THH)
- **Test** bit to enable the external testing of the pixel (1=test mode off, 0=test mode on)
- **Mask** bit to mask or unmask the pixel cell (1=unmasked, 0=masked)

The PRC is set by latching eight bits of the SR/C as indicated in fig. 2.8.

<table>
<thead>
<tr>
<th>b1</th>
<th>b2</th>
<th>b3</th>
<th>b4</th>
<th>b5</th>
<th>b6</th>
<th>b7</th>
<th>b8</th>
<th>b9</th>
<th>b10</th>
<th>b11</th>
<th>b12</th>
<th>b13</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Bit2 High</td>
<td>Bit1 High</td>
<td>X</td>
<td>Bit2 Low</td>
<td>Bit1 Low</td>
<td>Bit 0 Low</td>
<td>Test Bit</td>
<td>Mask Bit</td>
<td>Bit 0 High</td>
</tr>
</tbody>
</table>

Fig. 0.29 - Disposition of the PCR bits within the SR/C.

The default PCR value is then (111111x11xxxx)₂.

### 2.1.2.3 Pixel layout

The pixel layout uses 6 metal layers [Llo07]:
- Metal 1-2 are used for local routing inside the pixel
- Metal 3 is mainly used for the global routing: analog column biasing and digital control lines.
- Metal 4-5 are used for the analog/digital power distribution
- Metal 6 is used for the bump-bonding connection.

In Figure 2.9 the layout of the pixel cell is shown where the most important blocks are indicated. The octagonal bump bond opening, with a diameter of 20 µm, is placed on top of the analog side and is the input node of the CSA using the top metal.
2.1.3 The Medipix2 periphery

The Medipix2 periphery (fig. 2.10) circuitry provides the analog biasing and generates the digital control signals to the pixel matrix. It houses the 127 bonding pads for the chip connection, the bias DACs and the I/O control logic.

The 256-bit Fast Shift Register (FSR) performs the de- / serialization of I/O data while 14 DACs are used to tune the different bias values for the analog section of the pixel matrix.
Fig. 0.31 - The Medipix2 periphery floor plan. On blue the periphery blocks and IO lines using the analog power supply, on green the blocks and IO lines using digital power supply and on purple the blocks and IO lines using LVDS power supply (from [Llo07]).

2.1.3.1 The End-of-Column logic

The End-of-Column (EoC) logic (2.11) is the interface circuit between the pixel matrix and the periphery. There is one EoC block at the end of each pixel column. Each EoC includes sequential logic composed of a flip-flop with control logic and a digital buffer block for the global control signals ($CLK_{READ}$, $CONF$ and $SHUTTER$). The EoC flip-flops are linked together to form a 256-bit fast shift register (FSR) which constitutes the I/O data channel. For safety, two independent and identical FSRs (externally selectable through the $SPARE_{FSR}$ input line) are implemented. The read clock ($CLK_{READ}$) frequency is 256 times slower than the input clock ($FCLOCK_{IN}$) when data are transferred serially, and 8 times slower when either resetting or reading out the matrix in parallel. While reading out in parallel the 256 EoC blocks are divided into 32 subsections of 8 columns width (“super-column”) where each subsection is connected to one of the 32 lines of the parallel CMOS output bus.
Fig. 0.32 - Schematic of the EoC logic (only four blocks are depicted). The EoC flip-flops data lines are daisy-chained to form the FSR.

2.1.3.2 The LVDS I/O drivers

The Medipix2 chip exploits high-speed LVDS receivers and drivers as serial communication link. The position of the LVDS drivers/receivers (fig. 2.10) in the chips supports the daisy-chain connection between adjacent chips, minimizing the dead area between them.

There are three LVDS input/output signals at the left and right lower corners of the chip (fig. 2.12):

- **FCLOCK_IN** (in) is the master clock;
- **FCLOCK_OUT** (out) is the mirror of the master clock with a phase shift (~ 6 ns) due to the propagation delay into the chip. It is synchronous with **DATA_OUT**;

Fig. 0.33. The MDpx2 pinout of LVDS lines on the left and right lower corners of the chip.
- **DATA_IN** (in) is the data input line (set as rising edge of **FCLOCK_IN**);
- **DATA_OUT** (out) is the data output line (set as rising edge of **FCLOCK_OUT**);
- **ENABLE_IN** (in) starts the selected operation when goes low (usually should be reset to high state when the operation is finished);
- **ENABLE_OUT** (out) signals the end of the selected operation with a high-to-low transition.

The **ENABLE_IN** and **ENABLE_OUT** lines are available also as CMOS single-ended CMOS signals (fig. 2.12)

### 2.1.3.3 The bias DACs

The periphery area includes 13° 8-bit DACs which provide the voltage / current bias to the analogue and digital circuitry within the pixel cells. Each DAC has a unique identifier code used to select it. It is possible to either monitor the output voltage of a selected DAC through the **DAC_OUT** output pin or impose an external DAC value for the selected DAC through the **EXT_DAC** input pin. The 118-bit DAC register is written via the LVDS serial port and the FSR. It stores the 8-bit configuration byte of the 13 DACs, the 4-bit DAC identifier code, and the value of the “senseDAC” and “extDAC” flag bits which are used to enable the readout of an internal DAC voltage and the external voltage input, respectively.

Two external supplies are used to generate the reference current for the DAC LSB (**VDDA** and **DACBIAS**). Following a reset of the chip (see § 2.1.3.4) the output of each DAC provides a nominal setting corresponding to its mid-range binary value 10000000₂ (= 128₁₀).

The list of the 13 **MDFX2** DACs is reported in Table 2-I together with the DAC codes and the reference voltage/current values.

---

*The 14° DACs (IKRUMDISCHALF) is read-only so usually it is not considered.*
Table 0-I. List of the 13 Medipix2 internal DACs [Lio07].

<table>
<thead>
<tr>
<th>Pixel cell circuit</th>
<th>DAC name</th>
<th>Type</th>
<th>DAC code</th>
<th>Polarity</th>
<th>Range</th>
<th>External voltage(def.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSA</td>
<td>PREAMP</td>
<td>I</td>
<td>0011</td>
<td>e/h⁺</td>
<td>0 - 1.4μA</td>
<td>983 mV</td>
</tr>
<tr>
<td></td>
<td>IKRUM</td>
<td>I</td>
<td>0111</td>
<td>e/h⁺</td>
<td>0 - 30 nA</td>
<td>1537 V</td>
</tr>
<tr>
<td></td>
<td>FBK</td>
<td>V</td>
<td>1010</td>
<td>e⁻</td>
<td>0.4 - 0.85 V</td>
<td>600 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>h⁻</td>
<td>1.3 - 1.9 V</td>
<td>1.6 V</td>
</tr>
<tr>
<td></td>
<td>GND</td>
<td>V</td>
<td>1101</td>
<td>e/h⁺</td>
<td>0.9 - 1.3 V</td>
<td>1.1 V</td>
</tr>
<tr>
<td>Discriminator</td>
<td>DISC</td>
<td>I</td>
<td>0010</td>
<td>e/h⁺</td>
<td>0 - 1.67 μA</td>
<td>817 mV</td>
</tr>
<tr>
<td></td>
<td>THS</td>
<td>I</td>
<td>0101</td>
<td>e/h⁺</td>
<td>0 - 51.8 nA</td>
<td>1.425 V</td>
</tr>
<tr>
<td></td>
<td>SETDISC</td>
<td>I</td>
<td>0100</td>
<td>e/h⁺</td>
<td>0 - 400 nA</td>
<td>728 mV</td>
</tr>
<tr>
<td></td>
<td>THL</td>
<td>V</td>
<td>1011</td>
<td>e⁻</td>
<td>0.6 - 0.85 V</td>
<td>722 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>h⁺</td>
<td>1.2 - 1.6 V</td>
<td>1.425 V</td>
</tr>
<tr>
<td></td>
<td>THH</td>
<td>V</td>
<td>1100</td>
<td>e⁻</td>
<td>0.6 - 0.85 V</td>
<td>722 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>h⁺</td>
<td>1.2 - 1.6 V</td>
<td>1.425 V</td>
</tr>
<tr>
<td></td>
<td>DDL</td>
<td>I</td>
<td>0001</td>
<td>e/h⁺</td>
<td>0 - 50 nA</td>
<td>431 mV</td>
</tr>
<tr>
<td>Analog Buffer</td>
<td>ABUFFER</td>
<td>V</td>
<td>1110</td>
<td>e/h⁺</td>
<td>0.7 - 1.1 V</td>
<td>900 mV</td>
</tr>
<tr>
<td>LVDS driver</td>
<td>LVDSTX</td>
<td>I</td>
<td>0110</td>
<td>e/h⁺</td>
<td>0 - 580 μA</td>
<td>1.49 V</td>
</tr>
<tr>
<td></td>
<td>REFVVDSTX</td>
<td>V</td>
<td>1001</td>
<td>e/h⁺</td>
<td>0 - 1.1 V</td>
<td>1.04 V</td>
</tr>
</tbody>
</table>

As there is a unity gain voltage amplifier at the DACOUT pin only voltages are measured. The default values expected at DACOUT pin are reported in Table 2-I.

2.1.3.4 The IO control logic

The chip operation mode (Table 2-II) is controlled by means of six input signals named (in hierarchical order) reset, SHUTTER, P_S, M0, M1 and Enable_IN. All the operation, except the “chip reset” and the “acquisition” ones, are synchronous with the master clock (FCLOCK_IN). In order to perform anyone of the synchronous operations, the user should first set the control signals and after force down the Enable_IN signal to start the operation. The end of the operation happens when the Enable_OUT signal goes low.

The reset signal is used to control the Chip Reset (asynchronous) operation. When the reset pin is s low:

- The LVDS drivers/receivers are not active;
- The FSR is set high;
- All IO counters are reset to default values;
- All DACs are set to the mid-range value;
- The Dout[31:0] bus is in Hi-Z state. When reset is kept high, the other operations can be performed depending on the control signals setting as follows.

If shutter goes low the chip starts to count (asynchronous acquisition operation) until the signal goes back in high state. During the acquisition no other operation are available (except the reset of the chip).

Being reset and shutter both high, M0 and M1 set the operation mode:

- if M0 = 0 and M1 = 0, the Readout operation is selected. The contents of the pixel counters can be read out through either the LVDS serial line (“serial readout”) or the 32-bit parallel CMOS bus (“parallel readout”) depending on the status of the P_S signal; if P_S is low the serial mode is selected while in the opposite case (P_S high) the parallel mode is enabled. The readout is synchronous with the master clock signal (FCLOCK_IN) and starts when ENABLE_IN goes low. After data readout it needs to rebuilt the original 13-bit pseudo-random value of each pixel from the flow of bits delivered by the Medipix2 32-bit parallel bus and then to convert pseudo-random values to the corresponding binary ones through a LUT.

- if M0 = 0 and M1 = 1, the matrix configuration can be loaded through the serial input (DATA_IN). The matrix configuration is synchronous with the master clock signal (FCLOCK_IN) and starts when ENABLE_IN goes low. It needs 951976 (256x256x13 + 8 dummy bit) clocks to complete the operation.

- if M0 = 1 and M1 = 0, the DACs configuration can be loaded through the serial input (DATA_IN). The DACs setting operation is synchronous with the master clock signal (FCLOCK_IN) and starts when ENABLE_IN goes low. It needs 256 (+ 8 dummy) clocks to complete the operation.

- if M0 = 1 and M1 = 1, the Matrix reset operation can be accomplished. Reset of the matrix set all the counter bits to 1. It should be carried out before the first acquisition. 28680 (26x13x8+8) clocks are needed to perform this operation.
The operation modes of the MDpx2 are summarized in Table II.

<table>
<thead>
<tr>
<th>OPERATION</th>
<th>M0</th>
<th>M1</th>
<th>ENABLE_IN</th>
<th>P_S</th>
<th>RESET</th>
<th>SHUTTER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip reset</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>Acquisition</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Serial readout</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Parallel readout</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Set the matrix</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>X</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Set DACs</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>X</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Reset the matrix</td>
<td>1</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Test the FSR</td>
<td>0</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

### 2.1.3.5 The test pulse injector

Each pixel contains an 8 fF injection capacitance connected in series with the CSA input (see Fig. 2.2) to simulate the charge injection from the detector by an external voltage pulse. The Test Pulse operation is used to test the functionality of the pixel front-end circuitry without the sensor, and also, to calibrate the entire active matrix. The test is switched on by setting the ENABLE_TPULSE line high, and it is individually selectable on pixel basis through the PCR bit TEST bit.

The voltage test pulse of known amplitude is stepped though the TEST_IN input pin onto the injection capacitance $C_{test}$ which acts as a differentiator injecting into the preamplifier an equivalent charge $Q_{test}$ of

$$Q_{test} = \frac{buf \cdot V_{TP} \cdot C_{test}}{q}$$
where $\alpha_{buf}$ is the gain of the injection test pulse buffers (~0.825), $V_{TP}$ is the injection test pulse voltage amplitude (from 0.8 to 2.2 V), $C_{test}$ is the on-pixel injection test capacitance (~8 fF), and $q$ is the electron charge ($1.6 \cdot 10^{-19}$ C).

Fig. 0.35. Shape of the input test pulse. The correspondence between the input voltage step and injected charges are reported for holes (left) and electron (right) acquisition modes. The rise and fall time of the input voltage step should be as small as possible and always smaller than the peaking time of the preamplifier (~150 ns).
2.2 The Medipix2MXR20 ASIC

In this section the upgraded version of the MDPX2 chip, called Medipix2MXR20, is described. The main motivation for the new design solutions are presented.

The stronger motivations that lead to a full redesign of the MDPX2 chip were in order of importance [Llo07]:

- The voltage DACs showed a relatively high temperature dependence and a non-optimal linearity.
- The analog buffers didn’t have a unitary gain response as expected so it was not possible to do an absolute calibration using injection test pulse.
- The pixel counter was re-initialized when the end of scale (8001 counts) was reached. This was a problem if the counter registered value had to be used as an absolute measurement.
- The measured pixel radiation hardness (~10 krad) was at least one order of magnitude lower than expected.

Other changes bringing more functionality and robustness to the chip were added. The Mpix2MXR20 chip uses the same commercial 0.25µm CMOS technology used by the Medipix2. The pixel pitch, floor plan and chip dimensions of the Mpix2MXR20 are identical than the Medipix2 to avoid redesign of sensor and bump bonding masks. Given that several readout systems existed the chip readout architecture was kept unchanged.

Many changes have been made in the pixel cell (§ 2.2.1) and in the periphery (§ 2.2.2).

2.2.1 The Medipix2MXR20 pixel cell

The pixel architecture concept is very much as the Medipix2 pixel cell (see Figure 2.15). The dimensions of the cell are unchanged. Each pixel has 529 transistors and a static analog power consumption comparable to MDPX2 (~ 8 µW).

The main functional difference comes from the counter depth and the overflow control logic. The 14-bit shift register in acquisition mode (SHUTTER low) has a
dynamic range up to 11810 counts (instead of 8001) with an overflow control logic that stops the pixel counter, by acting on the pixel shutter signal, when the counter value gets to the end of scale.
Fig. 0.36. The analog and digital section of the MDPX2MXR20 pixel cell.

The CSA architecture is almost identical as the MDPX2 one. The MpixMXR20 upgrades in the CSA are aimed to enhance the radiation hardness and to generate internally the \( \text{IKRUMHALF} \) current from the \( \text{IKRUM} \) DAC by means of a local current mirror. This helps to minimize the pixel to pixel output voltage offset.

The discriminator architecture is similar to the MDPX2 one (fig. 2.4): The 3-bit current DAC for threshold adjustment was slightly modified. The masking NAND gate was moved to the digital side at the input of the DDL. The new zero-crossing circuit (\( Zx \)) uses the same scheme as in MDPX2. The \( \text{ISET} \text{DISC} \) DAC has been removed.

The block diagram of the digital side shown in fig. 2.5 is the same for the Mdpx2MXR20 digital side. The only changes are in the Shift Register/ Counter block (SR/C) and in the PCR register.

The Mpix2MXR20 schematic of the SR/C block (fig. 2.16) adds an extra shift register bit and a 14-input NAND gate as overflow logic. In acquisition mode (shutter low) the counter has a dynamic range up to 11810 counts. The overflow control logic stops the counter by toggling the internal shutter to a high state if the counter value is 11111111111110b.
The configuration bits have the same functionality as for MDPx2 but order by which the bits are latched into the PCR is changed (fig. 2.17).

<table>
<thead>
<tr>
<th>b0</th>
<th>b1</th>
<th>b2</th>
<th>b3</th>
<th>b4</th>
<th>b5</th>
<th>b6</th>
<th>b7</th>
<th>b8</th>
<th>b9</th>
<th>b10</th>
<th>b11</th>
<th>b12</th>
<th>b13</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X</td>
</tr>
</tbody>
</table>

The new Mpix2MXR20 periphery (fig. 2.18) has the same dimensions as in Medipix2. It was upgraded to improve the chip temperature dependence, linearity, testability, readout speed and robustness.

The internal DACs were redesigned [Bal07] to improve the stability of their output values to temperature and DC power supply variations. A better temperature stability was achieved using an internal band-gap reference circuitry as a bias circuit to obtain a temperature stable voltage ~1.16V.
The Medipix2MXR20 has two 14-bit voltage DACs for precise setting of the global thresholds ($THL$ and $THH$) and eleven 8-bit current and voltage DACs. The 14-bit threshold DACs are made of a high linearity 10-bit DAC (“fine”) plus a 4-bit DAC (“coarse”) whose current outputs are summed into the same resistor to create the output voltage (see Figure 4.10).

**Table 0-III.** List of the Medipix2MXR20 DACs displaying type, bit size and output range for each one.

<table>
<thead>
<tr>
<th>DAC NAME</th>
<th>Type</th>
<th>Bits</th>
<th>DAC CODE</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{Preamp}$</td>
<td>I</td>
<td>8</td>
<td>0111</td>
<td>0-2 µA</td>
</tr>
<tr>
<td>$I_{Illum}$</td>
<td>I</td>
<td>8</td>
<td>1111</td>
<td>0-40 nA</td>
</tr>
<tr>
<td>$V_{FBK}$</td>
<td>V</td>
<td>8</td>
<td>1010</td>
<td>0-2.2 V</td>
</tr>
<tr>
<td>$V_{GND}$</td>
<td>V</td>
<td>8</td>
<td>1101</td>
<td>0-2.2 V</td>
</tr>
<tr>
<td>$I_{Disc}$</td>
<td>I</td>
<td>8</td>
<td>1011</td>
<td>0-1.67 µA</td>
</tr>
<tr>
<td>$I_{THS}$</td>
<td>I</td>
<td>8</td>
<td>0001</td>
<td>0-51.8 nA</td>
</tr>
<tr>
<td>$V_{THL}$</td>
<td>V</td>
<td>14</td>
<td>0110</td>
<td>0-2.2 V</td>
</tr>
<tr>
<td>$V_{THH}$</td>
<td>V</td>
<td>14</td>
<td>1100</td>
<td>0-2.2 V</td>
</tr>
<tr>
<td>$I_{DelayN}$</td>
<td>I</td>
<td>8</td>
<td>1001</td>
<td>0-500 nA</td>
</tr>
<tr>
<td>$I_{BuffA}$</td>
<td>I</td>
<td>8</td>
<td>0011</td>
<td>0-10.2 µA</td>
</tr>
<tr>
<td>$I_{BuffB}$</td>
<td>I</td>
<td>8</td>
<td>0100</td>
<td>0-3.91 µA</td>
</tr>
<tr>
<td>$I_{LVDS}$</td>
<td>I</td>
<td>8</td>
<td>0010</td>
<td>0-3.92 µA</td>
</tr>
<tr>
<td>$V_{RefLVDS}$</td>
<td>V</td>
<td>8</td>
<td>1110</td>
<td>0-817 mV</td>
</tr>
</tbody>
</table>
As in Medipix2, the output voltages of each DAC can be monitored through the DACOUT output analog pin or externally forced through the ExtDAC input pin. For debugging purposes three internal voltages from the band-gap biasing circuitry as shown in Table 4.2.

Table 0-IV. List of the internal nodes which can be monitored through the DACOUT pin.

<table>
<thead>
<tr>
<th>Internal Signal</th>
<th>DAC CODE</th>
<th>Expected Value</th>
<th>Signal description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BiasDAC</td>
<td>0000</td>
<td>1.373 V</td>
<td>Voltage to be send to the gates of the transistors in the DAC array</td>
</tr>
<tr>
<td>BiasOutStage</td>
<td>0101</td>
<td>1.28 V</td>
<td>Voltage to bias the high swing output stage of some voltage DACs</td>
</tr>
<tr>
<td>VbgOnChip</td>
<td>1000</td>
<td>1.16 V</td>
<td>Internally generated reference voltage</td>
</tr>
</tbody>
</table>

2.2.1.1 The test pulse injector circuit

The new analog pulse injector circuit includes improved unitary gain buffers and a 32-bit register (CTPR) that selects individually the pixel columns to test. The buffer biasing is controlled by means of the two current DACs I_BUFFA and I_BUFFB. The voltage to charge conversion at the pixel input node can be found as:

\[ Q_{\text{test}} = \frac{V_{\text{in}} V}{50000} \]

The Medipix2MXR20 includes a 32-bit column test pulse register (CTPR) to select which columns are tested simultaneously. Every bit selects 8 columns distributed uniformly every 32 columns (i.e. if bit 0 is active then pixel columns 0, 32, 64, 96, 128,160, 192 and 224 are selected). With this architecture the total coupling capacitance of the test pulse line can be reduced by a factor 32 if only one bit in the CTPR is selected (when all the CTPR bits are active the Medipix2MXR20 has the same behaviour as the Medipix2). The CTPR is loaded simultaneously with the DACs configuration at EoC [143:174].

2.2.1.2 The I/O control logic

Table 11 summarizes the contents of the FSR. In total there are 178 bits used out of the 256 FSR bits. When reading the FSR (Chip Identification) after a Reset the output 256bit register will give all the bits set to High but the chip identification bits <195:218> will show the fuses contents. When writing the 154 write bits will set the DACs settings (122 bits) and the CTPR (32 bits).
The operation modes were simplified (see Table 4.3). The Reset Matrix command is eliminated because the matrix can be reset by a dummy parallel or serial readout. At chip Reset the LVDS Drivers are not active, the 24 bit Chip ID is latched into the End-of-Column logic (EoC), the IO control logic is reset to the initial condition, all DACs are set to the mid-range value and the 32-bit DOUT bus is in HiZ. Mpix2MXR20

Table 0-VI. The Mpix2MXR20 operation modes.

<table>
<thead>
<tr>
<th>$M_0$</th>
<th>$M_1$</th>
<th>Enable IN</th>
<th>$P_S$</th>
<th>Shutter</th>
<th>Reset</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>$X$</td>
<td>$X$</td>
<td>$X$</td>
<td>$X$</td>
<td>$X$</td>
<td>0</td>
<td>General reset of the chip</td>
</tr>
<tr>
<td>$X$</td>
<td>$X$</td>
<td>$X$</td>
<td>$X$</td>
<td>0</td>
<td>1</td>
<td>Acquisition</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Read out the matrix (Serial)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Read out the matrix (Parallel)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>$X$</td>
<td>1</td>
<td>1</td>
<td>Write the matrix PCR</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>$X$</td>
<td>1</td>
<td>1</td>
<td>Write/Read EoC register</td>
</tr>
</tbody>
</table>
A laser-blown 24-bit register placed in the periphery identifies uniquely each Mpix2MXR20 chip. The 24-bit register contains 12 bits to identify the wafer number, 4 bits for the in-wafer horizontal coordinate (X), 4 bits for the in-wafer vertical coordinate (Y), and 4 dummy bits (fig. 2.19). After a chip reset (RESET pin is set low) the contents of the 24-bit register are loaded into the FSR[195:218] register and read out with the read FSR register command.

![Figure 4.12. Mpix2MXR20 fuses EoC register.](image)

**Fig. 0.40. The 24-bit code bits within the MDPX2MXR20 FSR.**

### 2.2.2

One of the milestone of the Medipix2 design was the capability to cover large area by tiling single chip together. The chip layout foresees 2xN pixel mosaic. Adjacent chip can be connected in daisy chain (fig. 2.).

Adjacent chips can be daisy chained by connecting the CMOS out enable line `ENABLE_OUTC`, and the LVDS `DATA_OUT` and `FCLOCK_OUT` lines of one chip to the corresponding `ENABLE_INC`, `DATA_IN` and `FCLOCK_IN` of the next chip in the chain (figs. 2.20 and 2.21). With such a scheme the same readout system can be used for one single chip or any multi-chip daisy chained structure. Of course, the access time increases as the number of the chips.
In the Medipix2 chip both input and output data were latched and set at the rising edge of $F_{CLOCK \_IN}$ and $F_{CLOCK \_OUT}$, respectively. Thus, in multi-chip daisy chained structures, it required to invert the phase of output clock signal $F_{CLOCK \_OUT}$ (i.e., by inverting the wires of the LVDS line). In the Medipix2MXR20 such an issue has been resolved by latching the input data (DATA_IN) at the rising edge of $F_{CLOCK \_IN}$ and setting the output data at the falling edge of $F_{CLOCK \_OUT}$.

### 2.2.2.1 The Medipix quad

Using the previous scheme, a 2x2 multi-chip module called **quad** has been realized (fig. 2.22). The Medipix2 quad has been successfully assembled to the same 300 μm high resistivity Si sensor using solder bump-bonding [Far07]. The total sensitive area achieved covers more than 8 cm$^2$ with 256k pixels.
Fig. 0.43. Section and top view schematic of the Medipix2 quad [Llo03].

Dead area between neighbouring chips is avoided because the electronic cells at the chip boundary are connected to larger sensor diodes. The pixels placed at the edge between 2 chips are 3 times wider to cope with the distance between diced chips. The inner corners are covered by pixels which are 9 times larger than the rest (figs. 2.23. and 2.24).

Fig. 0.44. Schematic of the sensor segmentation at the boundary between two adjacent chips. Boundary pixels has a three times larger area (55 μm x 165 μm) to avoid dead area [For03].
Fig. 0.45. Top view schematic of the sensor segmentation at the centre of the quad.
2.3 Chip-carrier boards for the Medipix2 chip

The Medipix2 are supplied mounted on a chip-carrier card, usually referred as “chipboard”, where the chip is glued and wire bonded. Different chipboards have been developed to hold single and quad chips. All of them, except one, support the serial readout mode and are delivered with a 68-pin VHDCI\(^\text{10}\) female plug as interface connector. A SCSI-5 cable can be used for the connection with the readout board.

- The “CERN single chipboard” has been the first chip carrier board developed at CERN for Medipix2 chip (fig. 0.46). It can hold a single chip and the overall dimension is ~ 8 x 5 cm\(^2\). The VHDCI connector is used for the communication and powering of the Medipix2 chip whilst a standard LEMO connector is dedicated to the high voltage connection.

![CERN single chipboard](image)

Fig. 0.46 - The CERN “single chipboard” with a single Medipix2 chip glued on. Dimension of the board is ~ 8 x 5 cm\(^2\).

- The “2 x 4 chipboard” is a 9-layer PCB developed at NIKHEF\(^\text{11}\) using the “multi-layer build-up” technology [For03]. It can hold up to eight tiled single

\(^{10}\) Very High Density Cable Interconnect.

\(^{11}\) National Institute for Nuclear Physics and High Energy Physics (Netherlands).
Medipix2 chips (or two quad devices) arranged as a 2x4 array. It houses mainly passive components (decoupling capacitors, resistors) except one analog multiplexer switch per chip to provide analog test input pulses to all pixels. Total dimension of the board is 5.3 x 11 cm².
Chapter 2 – The Medipix2 chip

Fig. 0.47 - The Medipix2 2x4 chipboard (by NIKHEF) with a quad detector (from [www01]). Total dimension of the board is 5.3 x 11 cm².

- The NIKHEF “quad chipboard“ is the latest version of the chip carrier board developed in NIKHEF (fig. ?). It is projected to accommodate one quad detector minimizing of the PCB dead space around the detector area. From the top it can be tiled without any dead space, from the sides the dead space is minimized to few mm. The dimensions of the board are 7.4 x 5.6 cm². A duralumin block is foreseen as wire bonds protection and cooling of the chip.

Fig. 0.48 - The NIKHEF “quad chipboard“. The overall size is 7.4 x 5.6 cm².
2.4 Readout Systems for the Medipix2 chip

In order to exploit the Medipix2 features, specific hardware and software setup are required. Among the collaboration member, several hardware devices has been developed (see section 3.) even though at present the two official readout systems are the MUROS2 [San03] and the MedipixUSB [Vyk06].

2.4.1 The MUROS 2 readout system

The MUROS2 (Medipix Re-Usable Readout System v. 2.1) is an interface card between the Medipix2 chip and an host PC, through a commecially available PCI card (DIO by National Instruments).

MUROS2 design is based on a fPGA that implements the data transmission between the chip and the PC, as well as the large part of the hardware to control the operation of the chip (fig. 2). In particular, two serializer/deserializer FIFOs are implemented in order to decouple the MUROS-PC communication from the MUROS-CHIPBOARD one.
The 32-bit interface with the PCI acquisition card is divided in two blocks. Sixteen bits are used for asynchronous control/status signals whereas the other 16 bits are used as bi-directional data bus.

The MUROS2 supports the serial readout mode. Such a choice makes easier the hardware interface with the Medipix2 as well as the layout of chip-carrier board, especially when more than one chip has to be controlled. MUROS2.1 can manage up to eight chip (two quad assembly) and is compatible with the Medipix2, Medipix2 MXR and Timepix chips. The Pixelman as well as the MediSoft4 [Mai03] programs can be used as software GUI.

Electrons and holes acquisition can be simulated by a test pulse generator, allowing the test of the electronic of the chip before bump bonding to a sensor.

Data rate up to 160 Mbit/s have been tested, allowing for a minimum readout time of 5.734 ms for single chip.

More details on MUROS can be found on the NIKHEF website [www01].
2.4.2 The MedipixUSB readout system

The MedipixUSB readout system is an interface card between the Medipix2 chipboard and an host PC, through the standard USB1.0 interface [Vyk06].

The main component of this system is the microcontroller ADuC841\(^\text{12}\) (by National Instruments) which controls the functionality of the entire interface. It also embeds an high speed 420 ksp 12-bit ADC and DAC. The µC firmware can be updated directly via USB cable.

The USB interface is managed by the useful FT245BM\(^\text{13}\) chip which is a USB to parallel FIFO adapter with a 8-bit wide CMOS data bus and simple read/write control/status signal set.

---

12 The ADuC841 is delivered by Analog Devices (www.analog.com)
13 The FT245BM is delivered by the FTD (www.ftdchip.com)
As USB standard device, this readout system can be connected to the PC (Hot-swap) and it is detected and configured automatically without restarting the computer (Plug&Play). The board can be bus-powered through the USB cable which provides 5 V supply (up to 500 mA) or by an external power line. The 2.2V power supply for Medipix2 chip is achieved by a DC–DC step-down regulator. A variable high-voltage (from 5 to 100 V) source, based on the MAX1932, is provided for the sensor bias.

The PCB is 4-layer layout with a very compact size (4.5 x 6 cm²). All the I/O connectors are arranged along the short sides of the board. Medipix2 chipboards can be plugged directly to the VHDCI female connector.

The maximum clock frequency is 20 MHz which allows a data rate up to ??? Mbit/s corresponding to ~5 frame/s.

![Image](image-url)

**Fig. 0.54** - The MedipixUSB readout system by IEAP Prague. Overall dimension (without box) is 4.5 x 6 cm².

This system is also characterized by the open system architecture which allows to add further analog and digital interface through the connection of mezanine PCB modules. For example, the spectrometric plug-in module enables to measure the energy of interacting charged particles (e.g. alpha particles) by sensing the current pulse on the bias supply line by a charge sensitive preamplifier [Vyk06].

More information about this project are available on the IEAP website [http://aladdin.utef.cvut.cz/ofat/others/USB_Interface/index.html](http://aladdin.utef.cvut.cz/ofat/others/USB_Interface/index.html). A detailed description of the board design can be found in [Vyk05].
2.4.3 Other Medipix2 readout systems

Besides the two official Medipix2 readout systems described above, other members of the collaboration provided different system to fit specific requirements.

- The MaxiPix system (ESRF, Grenoble-FR) is a high frame-rate detector (based on Medipix2) mainly targeted for synchrotron applications. It is based on the PRIAM (Parallel Readout Image Acquisition for Medipix) custom board and a PCI 64-bit/66MHz interface card connected to the host PC through a fast (2.0 Gbit/s) optical link. PRIAM is able to readout up to 5 chips simultaneously (in 290 μs at 100 MHz clock) exploiting the Medipix2 parallel bus. Besides the parallel mode, the serial readout is available too. Data from Medipix2 chips are stored in five fast 1-Mbit FIFOs and then read and processed by the on-board fPGA. Different layout chipboards are available for single, quad and 1x5 ladder detectors (fig.); they are connected to the PRIAM board by means of short (~5 cm) flat ribbon cables.

Fig. 0.55 - Block diagram of the PRIAM board.

The ESPIA 64-bit/66 MHz PCI standard card developed by SECAD under ESRF specifications is used as acquisition card for PC interface. It offers a fast

---

14 MaxiPix stands for Multichip Area detector for X-ray Imaging based on a photon-counting Pixel array.
15 European Synchrotron Radiation Facility
bi-directional optical link and a data rate up to 180 MB/s in DMA mode. The PRIAM board is connected to the PCI card via an optical link capable of up to 2 Gbit/s (or 250 MB/s). Up to four optical channels are foreseen to allow further improvement of acquisition rate.

The PRIAM readout system has been tested to run the Medipix2 chip up to 110 MHz allowing to readout 5 chips in 290 μs at 100 MHz clock. This system is reported to readout up to 1500 frame/s for single chip - or 300 frame/s for 5x1 ladder - with an exposure time of 400 μs (44% of dead time) [Pon07].

![Image](image1.png)

**Fig. 0.56 - The ESPIA PCI acquisition card by SECAD SA (Grenoble, FR)**

![Image](image2.png)

**Fig. 0.57 - The MaxiPix readout system (left) and the 5 x 1 chipboard (right).**

- **DEMAS** is a fast readout system (IFAE\(^\text{16}\), Barcelona) developed in the frame of the **Dear-Mama** (Detection of Early Markers in Mammography) project aimed at the development of a low-dose X-ray system based on CdTe or Si detectors.

\(^{16}\) Institute de Fisica d’Altes Energies.
coupled to photon counting electronics for mammography and osteoporosis [Chm06]. The DEMAS (Dear-Mama Acquisition System) system is based on parallel readout and has reported a measured frame rate of 500 frame/s (50% dead time);

![DEMAS readout system board](image)

**Fig. 0.58** - DEMAS readout system board

- The **PCP** project (INFN\(^{17}\) Cagliari, Napoli, Pisa) is an optical link based readout system for the Medipix2 quad with a target frame rate of 25 Hz aimed at fast computed tomography scanning [Mar07]. A detailed description of the PPC system can be found below in Chapter 4;

- The **Rapid Universal INterface** (RUIN) of IEAP\(^{18}\) in Prague is an ongoing readout system with USB 2.0 and Gigabit Ethernet interfaces, and one digital signal processor (DSP) as board master device [Pla08]. The USB2.0 full-speed device interface offers a transfer rate up to 480 Mb/s. The Medipix2 serial readout mode is used but the parallel mode is a foreseen feature. Different Medipix2 chipboards can be connected through different dedicated adapter boards. Data are de-serialized on hardware by a devoted circuitry based on an fPGA and elaborated by a DSP providing high level of flexibility and high performance for online data processing (threshold equalization, flat field correction, beam hardening correction, cluster analysis, etc.). The interface is equipped with large memory allowing stand-alone operation and is compatible with all the Medipix2 family (Medipix2, Medipix MXR, Timepix) and with the future Medipix3 chip.

\(^{17}\) Italian National Institute for Nuclear Physics.

\(^{18}\) Institute of Experimental and Applied Physics (Prague)
The RELAXd (High Resolution Large Area X-ray Detector) project by NIKHEF is devoted to realize a large area detector made of several four-side tilable independent modules tiled together (fig. 2.39).

Fig. 0.59 - Block diagram of the RUIN readout system; general (a) and detailed (b) views [Pla08].

Fig. 0.60 - Artwork of a 2.3 megapixel x-ray detector made of nine RELAXd modules.
Each sub-module holds one hybrid detector composed of a pixellated semiconductor sensor bump-bonded to four Medipix2 chips and is connected to the main acquisition board by means of a fast Gigabit Ethernet link (3 Gbit/s).

![Test chipboard for the RelaXd detector. One single chip is wire-bonded on the chipboard for test purpose (left); detail of the Gigabit controller board (right).](image)

In order to reduce the dead area between the modules, the Medipix2 chip layout have to be modified removing the wire bond connections giving a 4-side tilable. For this, very small (50µm diameter) vias are etched through the wire bond pads of the chip and routed on ball grid array contacts.

![Profile of the current Medipix2 quad assembly device connected by the standard wire-bond technology (left). Profile of the RELAXd module device connected by the solder BGA on the back-side of the Medipix2 chips after through silicon via (TSV) etching (right).](image)

Each submodule is connected to the main acquisition board by means of fast Gigabit Ethernet link (3 Gbit/s).

Other simple readout prototype systems mainly for test purposes were developed by INFN of Cagliari as reported in [Fan03] and [Fan05].
2.5 Summary

In the first part of this chapter the architecture and the features of the Medipix2 readout chip has been described. The excellent results and limits showed by the former Medipix1 chip both stimulated the design of the new ASIC MEDIPIX2. The MEDIPIX2 has 65536 pixels of 55 µm x 55µm. Each pixel has a CSA whose output is DC coupled to two identical discriminator branches that form an energy window discriminator. The total analog power consumption per pixel is less than 8 µW. The digital part of the pixel contains an 8-bit pixel configuration register, the discriminator logic stage and a 13-bit shift register which acts as pseudo-random counter during the acquisition.

The MEDIPIX2MXR20 is an upgraded version of the MEDIPIX2. The main changes in the pixel consist of: an improved tolerance to radiation, improved pixel to pixel threshold uniformity, and a 14-bit counter with overflow control. The chip periphery includes new threshold DACs with smaller step size, improved linearity, and better temperature dependence.

Its main limit of the MDPX2 is the small detection area which force to use multi-chip array. At present, the larger area detector based un Medipix2 chip is one developed for DEARMAMA project, followed by the MaxiPixel (5x1 array) area of ESRF and the quad assembly (CERN). Any case management of such as assemblies in never easy at design and layout levels due to the large number of signal to be routed on the PCBs, power supply lines and so on. Detection area remains a critical point for the most of real applications where detection area is a must. The RELAXd project (NIKHEF) is an attempt to overcome this actual limiting factor.

In the second part of the chapter a brief description on the existing readout systems for the Medipix2 chip has been reported. The MedipixUSB represents a very effective and compact solution while MUROS2 is a more complex but faster solution. Both exploit only the Medipix2 serial readout mode and the maximum frame rate for single chip is in practice below 100 Hz with the MUROS interface and about 4 Hz for the USB interface [Vyk08].
Large area device based on multi-chip arrays required new and faster readout interfaces. This is the why of the increasing number of new readout system (DEMAS, PRIAM, RUIN, etc.) in the frame of the Medipix collaboration.

The PPC readout system described in this PhD thesis is a further example of this trend. It does not aim to compete with the existing or under development readout systems but it would rather represent a further and alternative solution. A complete description of the PPC system is the subject of the next chapter.
2.5.1 Bibliography


Chapter 2 – The Medipix2 chip


Chapter 3

The PPC Imaging System

Abstract - An x-ray imaging acquisition system for digital projection radiography and CT applications has been developed. It is named PPC (Pixel Detector with Optical Parallel Read-out for Computer Tomography) and consists of three custom-designed electronic boards plus a PCI digital interface card to link the system to the host PC.

The imaging system exploits a direct-conversion hybrid detector based on the Medipix2 readout chip (Chapter 2) bump-bonded to a silicon sensor with an active area of about 9 cm$^2$ segmented in 512 x 512 square pixels with 55 μm side length.

The detector stage is connected to the host PC through an optical link which allows fast, reliable and long interconnection. The system has been designed to acquire at least 25 frame/s with 10 % of dead time. This chapter illustrates each one of the electronic boards composing the PPC system while the control software and the characterization tests will be the subject of the Chapter 4.

Overview picture of the PPC imaging system setup during test and development activity.
3 The PPC Imaging System

3.1 Preliminary design considerations

The PPC (Pixel Detector with Optical Parallel Read-out for Computer Tomography) readout system is aimed for Computed Tomography imaging (e.g. CT, SPECT methods). Due to its small sensitive area (about 3 cm x 3 cm) it is suitable for small-animal imaging or to investigate single-photon counting detectors in CT (breast CT). During a CT acquisition, the setup of detector and X-ray tube (gantry) usually rotates continuously around the specimen (i.e. the patient in clinical surveys). CT application usually requires detectors with high dynamic range and fast readout, and a long enough interconnection to allows the detector to rotate into the gantry. These are the main reasons why the design of the PPC system foresees a long interconnection based on optical fibers and a fast acquisition rate (> 25 frame/s, 10% dead time).

PPC system exploits an hybrid pixel x-ray detector based on the Medipix2 quad (Chapter 2). In order to satisfy the frame rate constraint, it is mandatory to use the parallel mode to readout the Medipix2 chip. The maximum readout frequency for the Medipix2 parallel readout achieved till now is about 100 MHz (PRIAM and MaxiPix systems) while for the serial readout is below 200 MHz with the Medipix2MXR.

The project of the PPC system started from the frame rate requirement which imposes several design constraints, as explained below.

Let’s consider the minimum frame rate (25 frame per second or fps) as reference value. The period of each frame $T_{frame}$ is equal to 40 ms. Frame period is made of the sum of the exposure time $T_{exp}$ plus the data readout time $T_{read}$ that is “dead time” because the acquisition is inhibited during the readout phase (chapter 2). For each frame it is possible to define the percentage of dead time as in the following formula:

$$\text{dead time (\%)} = \frac{T_{read}}{T_{frame}} \times 100 = \frac{T_{read}}{T_{acq}} \times \frac{T_{read}}{T_{read}} \times 100$$  \hspace{1cm} (eq. 1)
Considering now a 10 % of dead time per frame, the readout time should be $T_{\text{read}} = 4$ ms. So frame rate and dead time requirements suddenly impose a key constraint on the readout time that is the readout frequency.

Of course, for a fixed frame rate, larger dead time values allow for larger readout times and then lower readout frequencies. On fig. 1 the readout frequency needed to achieve a data rate of 25 fps is drawn as function of dead time percentage for parallel and serial readout modes. Using the serial readout mode the frequency should be 1 GHz while only 31 MHz are required for parallel mode. At the same time, fixing the readout frequency, the serial readout mode will produce more noisy frame images due to the lower acquisition time.

![Readout frequency for 25 frame/s](image)

**Fig. 0.63.** Parallel readout and serial readout frequencies as function of the dead time percentage. Data are valid for an acquisition rate equal to 25 frame/s. The readout frequency should be equal to 1 GHz for serial readout and 31 MHz for parallel readout.

Now it should be consider the amount of data that corresponds to each frame. The Medipix2 quad matrix is made of 512x512 pixels, each of them having a 14-bit counter (Medipix2\textsubscript{MXR}2.0). So each frame corresponds to about 4 Mbit\textsuperscript{19} (512x512x14 = 3,670,016). The reading of 4 Mbit data in 4 ms requires a throughput of 1 Gbit/s or 125 MB/s.

\textsuperscript{19} The Medipix matrix is rounded to 4 Mbit to make easier the following calculations.
Fig. 3.1 shows that if we consider the serial readout mode, to obtain 25 frame/s with 10 % dead time it needs 1 GHz clock which is above the clock maximum rating. So if we consider serial readout clock up to 200 MHz, the dead time is always above 50 %. On the other side, the parallel mode requires a 31 MHz clock which can be considered a low frequency.

The frame rate is function of two parameters: the readout time ($T_{\text{read}}$) and the acquisition time ($T_{\text{acq}}$). Fig. 2 shows the relationship between the frame rate and the readout clock frequency for a fixed dead time percentage (equal to 10 %). In a similar way, fig. 3 shows how the frame rate changes when the dead time percentage varies and the readout clock is fixed (as actually happens in the PPC system).

![Plot of the frame rate as function of the readout clock frequency when dead time is fixed at 10 % (parallel mode is considered).](image)
The above arguments explain the reason why the Medipix2 parallel readout mode was chosen as main acquisition modality (the readout frequency is fixed and equal to 40 MHz) and show that for a complete comparison of the “frame rate” feature between different imaging system it is mandatory to declare the dead time percentage too. Of course this choice has several drawbacks as explained below.

As already mentioned, a long length connection between detector and host PC is suitable for CT applications if you want to move the detector around the specimen. Optical fiber link overcomes the limits of copper-wire interconnections offering long-length and fast data transfer medium and moreover featuring high noise immunity. The optical interconnection exploited in the PPC system is based on an optical link modular setup developed at the INFN section in Naples by prof. Alberto Aloisio and successfully integrated in the ATLAS muon chambers readout system (paragraph 3.?). This interconnections is capable of 640 Mbit/s transfer rate at 40 MHz clock. It

---

20 The serial readout mode is foreseen too for maintenance and test purposes.
21 In order to overcome this problem, some gantries take fixed the x-ray tube and the detector while the specimen rotates around itself. But such a designe cannot be always used.
guarantees a fast transfer of data from the motherboard to the *OptHub* (at least in 3 ms).

The readout system has to be controlled by an host PC thought a fast enough interface considering the previous explained frame rate requirement. The standard PCI interface was chosen because still today it is a reliable and widespread platform and because the previous knowledge of INFN Cagliari in PCI card development. A PCI 32bit/33MHz with DMA capabilities, obtained from the one described in [Fan06], was chosen as PC interface.

A new chip carrier board for the Medipix2 quad assembly was needed. Actually, among the chipboards developed by other collaboration members (CERN, NIKHEF), no one of them was designed for parallel readout.

At the same time, also a new motherboard card was foreseen to support the chip carrier card. Indeed, the 32-bit parallel output bus cannot be routed on a standard cable. It needs of driver/receiver buffers too. So a direct connection with the motherboard card was considered the straight solution.

Finally, the optical link system support was considered. Two solutions were examined. The first one, was based on the idea of a mezzanine card to be connected over the PCI board into the PC chassis. The second possibility consisted on a external adapter card, connected to the PCI card via a short flat cable. The last solution offered the advantage to share the same PC interface for more than one DAC system, multiplexing the data channel, acting as a “hub”.

Finally a custom Graphical User Interface (GUI) was developed to handle all the system operations through the host PC.

The image acquisition is consists of two consecutive phases:

1. **READOUT PHASE**: data are read out from the detector in quite less than 3 ms (at 40 MHz clock frequency) and stored in a FIFO memory;

2. **ACQUISITION PHASE**: data are moved from the FIFO toward the PC, going through the *OptHub* and the PCI card.

The readout phase is handled/accomplished by the *Motherboard* or fPGA which also provide to send the readout data to the *OptHub* through the optical link. Once data
are loaded on the OptHub FIFO an interrupt is generated to indicate that new data are ready. The software intercept the interrupt and start to acquire the image data through the PCI acquisition card.

When the readout phase is finished, suddenly begins the next exposure (if requested) and the acquisition phase starts. The acquisition phase have to be accomplished while the next exposure is started that is in no more than about 20 ms at least (considering the constraint of 25 fps, 10 % dead time). During this time is also possible to read more than one detector by multiplexing the OptHub card optical link.

The parallel readout implementation has a great impact on the PCB layout design. Beside the fast data transfer rate achievable with a parallel bus respect a serial one, serial communications protocols simplify data transfer over PCB traces (and cables) by narrowing data path and in turn reducing PCB layers, cable width and connector size and pins. Moreover differential signal standards (like LVDS) reduce EMI and eliminates the skew problems between parallel data and clock paths.
3.2 The PPC DAQ architecture

The PPC DAC architecture is depicted in Fig. 4b. It consist of:

- the chip carrier board, named Chipboard_4C;
- the main control board of the detector stage, named Motherboard_Opt;
- the Opt-hub card, which interface the optical link with the PC;
- the PCI9054 card, which interfaces the acquisition system with the host PC.

The first two cards form the detector stage. The clock frequency is 40 MHz for all the boards except the PCI one, which have a 50 MHz clock.

The design of all the system electronic cars is based on on-field programmable logic array (fPGA) devices. FPGAs have a flexible and programmable hardware architecture made of Configurable Logic Blocks (CLBs), surrounded by a perimeter of programmable Input/Output Blocks (IOBs). These functional elements are interconnected by a powerful hierarchy of versatile routing channels. FPGAs are customized by loading configuration data into internal static memory cells. Unlimited reprogramming cycles are possible with this approach. Stored values in these cells determine logic functions and interconnections implemented in the fPGA.
Configuration data can be read from an external serial PROM or written into the FPGA in Boundary Scan modes. Beside the versatility of a fast programmable solution, FPGA offers other benefits. These are ideal for shortening product development cycles and is a cost-effective solution for small volume production.

Spartan-IIE devices provide system clock rates beyond 200 MHz well above the boards clock frequencies. In addition to the conventional benefits of high-volume programmable logic solutions, Spartan-IIE FPGAs also offer on-chip synchronous single-port and dual-port RAM (block and distributed form), DLL clock drivers, programmable set and reset on all flip-flops, fast carry logic, and many other features.

Board layouts are mainly based on SMD package components to increase the packing capacity. Ball Grid Array (BGA) packages were avoided because the cost of soldering and because lead pin packages are more flexible for developing purpose.

At any given time a bus may be owned by a bus resource called bus master. Ownership allows the bus master to be the only resource executing bus cycles. A bus arbiter is needed to grant the bus ownership to only one master at time. Local Bus arbiter circuit is implemented into the CPLD.
3.3 The “Test setup”

Due to high complexity of the DAQ, a simplified design [Mar07] without the optical link stage was first considered (Fig. 4a). The aim was to make easier the develop and debug of the detector stage, (Motherboard\textsubscript{Test} plus Chipboard\textsubscript{4C} cards). In fact, with respect to the complete setup the test one shares both the PCI and Chipboard\textsubscript{4C} cards. The project of Motherboard card, referred as Motherboard\textsubscript{test}, is quite different because it is directly connected to the PCI card via a couple of flat cables but the interface with the Chipbard\textsubscript{4C} card is not affected by this. So a large part of design and layout of the Motherboard\textsubscript{test} card was used for the project of the more complex Motherboard\textsubscript{opt} card. As a final result, the test setup is now a complete readout system offering all the features of the complete DAQ except the optical link. The Motherboard\textsubscript{test} card will be described below while the other common cards will described later in another paragraph.

The main limit of the first Motherboard\textsubscript{test} is related to the absence of the buffer in the I/O control data channel. The maximum on-chip RAM available on the fPGA is 56 kbit, so it is not enough to store matrix configuration of a single Medipix2. This limits the speed of the matrix configuration operation because data have to be sent to the chip is small packet.

In the new Motherboard\textsubscript{TestMK} two 16-bit wide / 4-Mbit depth FIFOs (IDT’s 72V2113) has been inserted in the bi-directional control data channel, before the fPGA. Moreover an independent supply circuit is added to power the Chipboard\textsubscript{IC} card; two different linear regulator are used for provide the analog and the digital 2.2 voltage for the Medipix2 chip. The 8 (CMOS) GPIO are divided in two independent 4-bit groups which are configurable as input or output. In a similar way, four LVDS lines divided in two separate groups 2-bit can be used as input or output. One of this LVDS signal can be used for the PCI clock.
Fig. 0.66. PPC MotherboardMK card. The new Motherboard of test setup has a new independent power supply circuit per the Chipboard card, and two 16-bit wide / 4-Mbit depth FIFOs on the I/O control data paths.
3.4 The PPC-PCI9054 acquisition board

The PCI acquisition board is a general purpose digital acquisition board with a standard PCI 32bit/33MHz interface [Fan06]. It is based on the PCI9054 PCI bridge (by PLX Technology, Inc.) which provides a link between the PCI bus (protocol and signalling) and CMOS standard Local Bus. Two programmable logics, one fPGA and one CPLD both by Xilinx, are used to manage the data and control/status signals of the local bus. Up to 68 CMOS plus 4 LVDS lines routed on two 80-pin I/O header connectors (3M HE-81080) are available to interface outer devices. These I/O lines can be programmed as input or output by changing the fPGA hardware configuration. It allows high flexibility in designing the I/O interface so that the same card can fit different requirements.

The global reset pushbutton switch allows the user to reset the devices of the board.

Board layout is based on SMD components except the I/O header connectors which are through-hole type. All components are on the PCB top side as PCI recommendations.

![PCI card PCB layout (top side). The main parts of the board are pointed out for text reference. The PCB dimensions are 17.7 cm x 9.8 cm (PCI “standard” size).](image)

---

22 Peripheral Component Interconnect.
3.4.1 The PLX PCI9054 bridge

A bridge is simply a circuitry used to link different busses. Its primary purpose is to interface one bus protocol to another. The protocol includes the definition of the bus control signal lines, and data and address sizes. The PCI9054 bridge is an I/O interconnect device that allows to connect two different I/O bus architectures with one of them being PCI. In addition to being a local bus to PCI bus bridge, PCI9054 is also a “I/O Accelerator” that is a controller that allows the Local Bus to communicate directly with other devices on the PCI bus without going through the CPU. PCI9054 supports bus mastering (DMA) as a means of improved performance.

The PCI9054 bridge provides also the electrical interface with the PCI bus. In fact, PCI bus has well-defined electrical specifications. The PCI bus is designed to signal from one component to another with the “reflected wave” technique. When a signal is launched onto the bus, it is required to propagate to all extremes of the bus wire with only one half of the required logic threshold voltage amplitude. So the physical extremes of the bus wire are encountered, the signal reflects and propagates back to all points of the bus wire again. If the bus is implemented correctly, all points on the bus will obtain valid logic voltage threshold levels by the end of the second propagation. For this scheme to work properly, there must be enough instantaneous current from an output buffer to develop the initial half amplitude step on the bus. On the other hand, too much current will create excessive reflections and may require too much tie for the bus to settle. Thus the I/O buffers of PCI add-in cards must meet specific AC switching characteristics to comply with the PCI signaling requirements [Sol98].

The PCI9054 interfaces a PCI host bus to several Local Bus types. The local bus can directly interface specific CPU (e.g. Motorola) or a The PCI 9054 can be programmed to interfaces a PCI Host bus to specific CPU (mode M, mode J) or to set a general purpose non-multiplexed bus (mode C, 32-bit data bus / 32-bit address space).
Fig. 0.68. Block diagram of the PLX’s PCI9054 chip.

PCI9054 uses LHOLD (Out) and LHOLDA (In) signals to access the Local Bus; it asserts LHOLD to request control of the Local Bus while LHOLDA is asserted by the Local Bus arbiter (CPLD) to grant the Local bus to the PCI9054.

Direct Memory Access (DMA) is a technique for transferring blocks of data between system memory and peripherals without the intervention of a microprocessor (e.g. system CPU). Using this technique reduces load on the system processing elements, while enabling much higher data throughput versus using standard processor read and write transactions. Scatter-Gather DMA augments this technique by providing data transfers from on non-contiguous block of memory to another by means of a series of small contiguous block transfers. PCI9054 DMA Controller provides a master/slave interface, buffer descriptors, and two DMA channels.
3.4.2 CPLD

The Complex PLD (Xilinx’s XL9572X-7, TQ100\textsuperscript{23}) is used to generate control signal for the fPGA and SRAM modules. Referring to the hardware diagram (fig. 3.7), there are three main functional blocks inside the CPLD: “SRAM controller”, “Local Bus Arbiter” and “Chip Select generator”.

As SDRAM controller the CPLD manages the read/write operation on the two SRAM chips. During memory cycles, the SRAM controller generates all control signals, SRAM chip select (\texttt{SRAMCS\#}), SRAM output enable (\texttt{SRAMOE\#}) to the Synchronous SRAM. During burst memory cycles, the SRAM controller will latch the 15 starting address bits (when ADS\# is low) and use its built-in 11-bit internal address counter to advance the addresses to the synchronous SRAM. This effectively divides the SRAM into 16 “pages” of memory. It is important to note that the BTERM\# signal is not implemented in the SRAM controller, thus, software should take care not to have this counter overflow from 0x7FF to 0x000, lest the beginning locations of a given “page” be overwritten, on write cycles. A more appropriate method would involve generating a BTERM\# signal each time all 11 bits of the counter are 1’s, thus forcing the PCI 9054 to break up the burst and generate a new address cycle.

As Local Bus Arbiter the CPLD can grant the Local Bus to the PCI9054, fPGA depending on their request (depending on a priority scheme).

- Address decoder: the local address space can be divided in different areas by choosing a base address and a depth. The Local Address bus (LA[2:31]) is routed on the CPLD which can match the requested address and generate chip select control signals (depending on the ) to enable the access to one resource (fPGA, SRAM etc…)

The Chip Select Generator generate the enable signals for the fPGA and the SRAM. It’s a common practice when a communication bus is shared between more than one device (which can read and write data on that bus) to use chip select signals to avoid data collisions if more two or more devices access the bus at the same time. Also

\textsuperscript{23} 100-pin Thin Quad Flat Package.
during reading operation, the same address can correspond to different devices so it need to indicate which is the device to address. “Chip select” or “chip enable” signal are generate by a address decoder which divide the physical available space in two or more logical spaces. Each device is associated to una logical space and is enabled only when the physical address falls in the logical one. Of course, the sum of logical spaces cannot be bigger than the physical one. The address decode circuit is implemented into the CPLD, which is suited for such a hardware and offers a fixed timing patterns.

![Block diagram of the CPLD firmware](image)

- **Fig. 0.69.** Block diagram of the CPLD firmware

On the PCI 9054 side, the SRAM controller generates the active low ready signal (READY#) to terminate PCI 9054 memory cycles. The external arbiter in the CPLD accepts two Processor/Local Bus request signals, LBR[1:0], and the bus request from the PCI 9054 LHOLD signal, and it generates bus grant signals, LBG[1:0], to the Processor/Local Bus masters, and LHOLDA to PCI 9054 chip.
3.4.3 The fPGA data bus interface

The fPGA (Xilinx’s XC2S200E-PQ208\textsuperscript{24}) directly interface the Local Data bus (LD[31:0] signals) and controls all data transfers between the PCI board (Local Bus) and the outer periphery (I/O connectors). It implements a multiplexer/demultiplexer that switches between the data readout channel (32-bit) and the control data channel (16-bit input / 16-bit output) and the General-Purpose IO lines (GPIO). All this lines are directly routed to the IO header connectors. This fPGA offers high flexibility for future on-fly data handling (i.e. deserialization of Medipix2 readout data requires a 7168-bit depth FIFO, available in a XC2S300 E fPGA).

3.4.4 Serial EEPROM

A 2 Kbit serial EEPROM (Microchip’s 93AA56, 8-pin SMD) is connected directly to the PCI bridge and provides the configuration data to initialise the PCI 9054 after the system boot. The EEPROM stores 88 bytes of pre-programmed configuration data in the serial EEPROM, which include device and functional information for plug-and-play (PnP), PCI memory resource allocation, and initial values of internal registers.

3.4.5 Synchronous Static RAM

Up to 2x4-Mbit SRAM chips (CY7C1351F-100 (128K x 36) Flow-through) are available as data storage in the PCI card. SRAM takes 15 address lines (SA16-SA2)

\textsuperscript{24} 208-pin Plastic Quad Flat Package.
from the SRAM controller implemented in the CPLD. The data path is divided in four 8-bit channel but in actual configuration only 32-bit access are allowed (SRAM byte write enables \( \text{SRAM}_{\text{BW}}[3:0] \) are tied to ground). The data lines of the SRAM are directly connected to the PCI 9054 local data bus (LD31-LD0). During memory burst cycles, the SRAM performs continuous single read cycles or single write cycles. The SRAM controller (CPLD) does all the timing conversion and generates the address to the SRAM.

### 3.4.6 Clock generator circuit

The clock generator is based on a 50-MHz small package crystal oscillator (Jauch Quartz’s VX3MH5000) and one clock buffer (Cypress’s CY2305-1H-SO8 \(^{25} \)) that fan out the clock signal from the oscillator into 5 clock signals with zero delay (< 350 ps input-to-output propagation delay) and very low skew (< 250 ps output-to-output skew) between the outputs. The clock buffer outputs drive the PCI 9054 bridge, the fPGA, CPLD, and the SRAM. The fifth output is connected to a CMOS-to-LVDS driver and can be used to send the PCI board clock to outer periphery.

The clock lines are properly terminated near the receiver device with a configurable termination circuit (fig. ) in order to limits reflections. Serial, parallel and AC termination schemes are possible.

---

\(^{25}\) 8-pin Small Outline package
3.4.7 Power supply circuit

The power supply circuit is based on two low drop linear voltage regulators with 3.3 V / 1.5 A (LD1086D2T33-D^2PAK^26) and 1.8 V / 1 A (REG117A-1.8) outputs. The input voltage is 5 V and is supplied by the host PC through the PCI bus connector. The output lines are ... by an EMI filter (Murata's NFM41P). Bypass and sink capacitors are distributed throughout the board to give clear and stable supply. Two power LEDs located at the top edge of the board indicate the presence of the board supply voltages. The maximum power allowed for any PCI board is 25 W, even if power consumption up to 10 W is recommended [PCI specifi]. Anycase the maximum card power dissipation is encoded on PRSNT1# and PRSNT2# pins of the PCI expansion card.

3.4.8 Reset circuit

A reset/supply supervisor IC (Maxim’s MAX6306UK30D1, SOT23-5^27) monitors the power supply and asserts a global reset to reset all the board devices. A start-up, it imposes a power-on-reset period of 1 ms. In addition the global board reset can be generated manually through pushbutton switch.

---

^26 5-pin Small Outline Transistor package.
3.4.9 I/O connectors

Two 80-pin header connectors (3M’s 81080) are foreseen as hardware interface with outer devices. Contact pins are through-hole to save space and are disposed on two rows tail. One contact tail is tied to ground. For each connector 36 contacts are dedicated to single-ended lines, 4 contacts are for two differential lines and the residual pins are tied to ground in order to improve the noise immunity on the flat-cable (fig. ?). Chips resistor arrays are foreseen for all single-ended signals for cable parallel termination.

![Diagram of I/O connectors](image)

Fig. 0.73. Draft of flat cable layout used to connect the PCI card with outer devices. Data wires are interleaved with grounded wires to reduce cross-talk between neighbouring wires.

Fig. ? shows the propagation delay of the output signal d0 going from the PCI card to the Motherboard card through a 50 cm length flat cable. As expected, the propagation delay for 0-to-1 transition (~3.7 ns) is a bit higher than the 1-to-0 transition (~3.4) is mainly due to the CMOS driver. In fact, in digital CMOS rise time is usually slower than fall time.

![Graph of propagation delay](image)

Fig. 0.74. Measure of the propagation delay through the flat cable for 0-to-1 (left) and 1-to-0 (right) transitions. Data are taken on the PCI card at the FPGA output pin D0 (upper trace) and on the...
Motherboard at the corresponding FIFO input pin (lower trace). Propagation delay is about 3.7 ns for the 0-to-1 transition and about 3.4 ns for the 1-to-0 one. The length of the flat cable was 50 cm.

3.4.10 PCB layout

The PCI9054 card PCB was manufactured by Baselectron factory (Pavia, IT) in 8-layer PCB with following stack:

1. Routing
2. Power (3.3 V, plane layer)
3. GND (plane layer)
4. Routing
5. Power (1.8 V, plane layer)
6. Routing
7. GND (plane layer)
8. Routing

The PCB is compliant with “short universal” layout with dimensions 17.4 cm x 10.7 cm (see “Mechanical Specifications” in [PCI2.2])
Fig. 0.75. PCI card layout (screenshot from OrCad Layout)
4 The PPC-PCI9054 acquisition board

As already mentioned at the beginning of this chapter, the optical link interconnection used in the PPC system was developed by prof. Alberto Aloisio (University and INFN of Naples) for the Level-1 Muon Trigger of the ATLAS experiment at LHC [Alo06]. In fact, the PPC optical link only differs from the previous one for a few design changes.

The optical link stage can be thought of as a “virtual ribbon cable” interface for the transmission of data and control words. A parallel word loaded into the Tx (transmitter) chip is delivered to the Rx (receiver) chip over a serial channel (optical link) and is then reconstructed into its original parallel form.

The PPC optical link setup is based on three different open frame module designed to be used as a mezzanine module on the master board:

- The **TRX module** is a 16-bit half-duplex transmitter/receiver unit;
- The **RX2 module** is a 32-bit simplex receiver unit;
- The **TX2 module** is a 32-bit simplex transmitter unit.

![Block diagram of 32-bit simplex (left) and 16-bit half-duplex combinations.](image)

The TX2 and RX2 modules are coupled in order to implement a simplex 32-bit data channel while a TRX pair is used for the 16-bit half-duplex channel (fig. 15) for data/status/control signals transmission. Moreover a clock in phase with the received parallel data is extracted from the serial data stream. Transmitter and receiver chips are able to detect any loss of synchronization between them and to resynchronize themselves in a few clock cycles.

The **HDMP 103xA** Serializer/Deserializer (SERDES) chipset transparently translates a 16-bit parallel bus into a PECL serial stream with embedded clock information. This single serial stream simplifies transferring a 16-bit bus over PCB
traces and cables by eliminating the skew problems between parallel data and clock paths. It saves system cost by narrowing data paths that in turn reduce PCB layers, cable width, and connector size and pins.
4.1.1 The RX2/TX2 and TRX modules

The optical link modules are small interface cards (8 cm x 5.2 cm) based on the HDMP 103xA chipset and the HFBR 5912 MT-RJ Fiber Optic Transceiver both by Agilent Tech. The HDMP 103xA chipset consists of the HDMP-1032A transmitter and HDMP-1034A receiver chips which can be combined to build a high-speed serial data link for point-to-point communication. The HDMP-1032A is a 16-to-1 bit serializer while HDMP-1034A recovers the serial stream and converts it in a 16-bit word. The HFBR 5912E is a small form factor MT-RJ fiber optic transceivers for Gigabit Ethernet connections. It converts a serial stream from electrical to optical form. Together with the HDMP 103xA chipset implements an optical communication channel.

The G-Link standard uses Conditional Inversion with Master Transition (CIMT) data coding scheme. The CIMT serial stream consists of a user-selectable 16 or 20-bit payload (D-field) followed by a 4-bit coding field (C-field). The C-Field value labels the payload as a data word, a control word or an idle word, which is transmitted to keep the link synchronized when no user data/control are available. The protocol

---

28 Now distributed by Avago Tech. (www.avagotech.com)
29 Mechanical Transfer Registered Jack
guarantees a logic transition in the middle of every C-Field (the so-called Master Transition) which is used by the receiver unit as a fixed time-stamp.

An extra 17<sup>th</sup> bit (“flag bit”) can be sent together with the data word if the \texttt{FLAGS} is asserted. A user control space is also provided. It \texttt{TRG}_T\texttt{X} is asserted on the Tx chip, the least significant 14 bits of the data bus will be sent and the \texttt{TRG}_R\texttt{X} line on the Rx chip will indicate the data is a control word.

The \texttt{TX2} / \texttt{RX2} modules house two HFBR 5912E tranceiver driven by two HDMP-1032A transmitters (\texttt{TX2}) or two HDMP-1034A receivers (\texttt{RX2}). The parallel data interface is TTL, 32-bit input for \texttt{TX2} and output for \texttt{RX2}.

On the TRX module both one 1032A transmitter and one HDMP-1034A receiver with the HFBR 5912E tranceiver. The parallel data interface is 16-bit input + 16-bit output. (input for \texttt{TX2} and output for \texttt{RX2}). A flag bit is also present and can be used as an extra 17<sup>th</sup> bit under the user’s control. A 16-bit parallel word loaded into the Tx (transmitter) chip is delivered to the Rx (receiver) chip over a serial channel and is then reconstructed into its original parallel form. Each module requires a 3.3 V (1 A max) power supply and a clock frequency of 40 MHz. Useful control/status flag are provided as summarized in Table VII.

<table>
<thead>
<tr>
<th>Signal name</th>
<th>Input/Output</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D_TX[0:15]</td>
<td>In</td>
<td>Data input port of the TRX module</td>
</tr>
<tr>
<td>Q_RX[0:15]</td>
<td>Out</td>
<td>Data output port of the TRX module</td>
</tr>
<tr>
<td>D_TX2[0:31]</td>
<td>In</td>
<td>Data input port of the TX2 module</td>
</tr>
<tr>
<td>Q_RX2[0:31]</td>
<td>Out</td>
<td>Data output port of the RX2 module</td>
</tr>
<tr>
<td>CLK40</td>
<td>In</td>
<td>Input clock for TRX / RX2 / TX2. Used to generate the high speed serial clock</td>
</tr>
<tr>
<td>CLKOUT</td>
<td>Out</td>
<td>PLL recovered clock (only from RX2 and TRX receiver section)</td>
</tr>
<tr>
<td>PASSRX</td>
<td>In</td>
<td>Parallel Automatic Synchronization System (PASS) allows receiver to read recovered words with local reference clock.</td>
</tr>
<tr>
<td>LOCKTX</td>
<td>Out</td>
<td>When asserted (high) indicates that the Tx PLL achieves frequency lock to the CLKTX</td>
</tr>
<tr>
<td>TRGTX</td>
<td>In</td>
<td>When \texttt{TRG}_T\texttt{X} is asserted, 14-bit words are transmitted and labelled as “control” word</td>
</tr>
<tr>
<td>TRGRX</td>
<td>Out</td>
<td>The \texttt{TRG}_R\texttt{X} flag indicates that a “control” word is available at the Rx chip output bus</td>
</tr>
<tr>
<td>DAVTX</td>
<td>In</td>
<td>When \texttt{DAV}_T\texttt{X} is asserted (and TRG is de-asserted), 16-bit words are transmitted and labelled as “data” word</td>
</tr>
</tbody>
</table>
Table 3.1 - Summary of DA V旗 and RX output values

<table>
<thead>
<tr>
<th>DA V</th>
<th>RX</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Out</td>
<td>The DA V flag indicates that a “data” word is available at the Rx chip output bus</td>
<td></td>
</tr>
<tr>
<td>Flag Ent</td>
<td>In</td>
<td>When asserted, the flag bit Flag Tx bit input is sent as an extra 17th data bit (only during “data” word transfer). Flag Ent and Flag Ent must be both asserted</td>
</tr>
<tr>
<td>Flag Rx</td>
<td>In</td>
<td>When asserted, the flag bit is available at the Flag Rx output</td>
</tr>
<tr>
<td>Flag Tx</td>
<td>In</td>
<td>“Flag bit” input pin (Flag Ent must be asserted)</td>
</tr>
<tr>
<td>Flag Rx</td>
<td>Out</td>
<td>“Flag bit” output pin (Flag Ent and Flag Ent must be both asserted)</td>
</tr>
<tr>
<td>Ready Rx</td>
<td>Out</td>
<td>When asserted indicates that no errors on data are recognized</td>
</tr>
<tr>
<td>Error Rx</td>
<td>Out</td>
<td>When asserted indicates that the word received are invalid data</td>
</tr>
<tr>
<td>Sd Rx</td>
<td>Out</td>
<td>When high, indicates if the link is functional or a definite optical fault occurs (e.g. unplugged connector, broken fiber, or failed far-end transmitter or data source)</td>
</tr>
<tr>
<td>L E</td>
<td>Out</td>
<td>When low, enable the optical transceiver (HFBR-5912) Tx laser</td>
</tr>
<tr>
<td>I2c Scl</td>
<td>In</td>
<td>I²C bus clock</td>
</tr>
<tr>
<td>I2c Sda</td>
<td>In/Out</td>
<td>I²C bus data</td>
</tr>
<tr>
<td>I2c A[0:1]</td>
<td>In</td>
<td>Address for the I²C chip (AD7417)</td>
</tr>
</tbody>
</table>

A temperature sensor (Analog Devices’ AD7417R, 8-pin SSOP30) with I²C serial interface is provided to monitor the optical transceiver temperature.

On the bottom side, two high-density low-profile SMT socket (Robinson Nugent’s P08-100SL-A-G, 100-pin DIL 0.8 mm pitch) are used as mechanical interface with the driver board while the optical fiber is connected directly on the HFBR tranceiver through an MT-RJ connector.

![Fig. 0.77. Picture of the TRX and RX2 optical link modules.](image)

30 Standard Small Outline Package.
Chapter 3 – The PPC Imaging System: the optical link interconnection

The optical modules require nominal 3.3 V / 1A power supply. Characterization tests have shown that the HDMP1032A serializer chip requests a slower voltage (about 3.2 V or less) to properly work. So the transmitter section of the TRX and the TX2 circuit should be powered by adjustable regulators to match the correct supply voltage.
5 The “OptHub” card

In order to support the optical link modules at the host PC side, the PPC architecture foresees an Optical-to-Electric (O/E) interface board, named Opt-Hub. The word “hub” means that this board should allow the connection of more than one detector stage to the same PCI board.

The OptHub is connected to the PCI9054 card by means of two 80-wire high density (0.5” pitch) flat cables. One of them is configured as bi-directional channel (16-bit wide input plus 16-bit wide output) for control and data communications while the second one is configured as unidirectional (from OptHub to PCI9054) 32-bit wide channel for readout data coming from the detector stage. Each data channel is buffered and 4-Mbit depth FIFOs are provided to decouple the communication busses between the OptHub and PCI9054 cards.

The OptHub card holds the TRX and RX2 optical modules to translate in optical kind signal the 16-bit half-duplex and the 32-bit simplex data channels already mentioned. Three optical fibres are needed to link the OptHub to the detector stage.

The Opt-Hub card exploits a small size fPGA (Xilinx’s XC2S100E-TQ144) as master controller devices to manage the optical modules and the FIFO chips. All active devices works at 40 MHz clock frequency. The board requires two +5 V / 2 A supplies, one for them being dedicated to the optical modules.

The current release is to be intended as a preliminary test bench board for the optical modules and does not yet work as hub. The first PCB with dimensions 16 cm x 18 cm but a more compact layout (10 cm x 20 cm size) is ongoing.
Fig. 0.78. The PCC Opt-Hub card (rev. 0).

5.1 The Opt-Hub architecture

The Opt-Hub card represents the optical to electric (O/E) interface between the PCI9054 card external bus and the optical medium. Its main purpose is to support the TRX and RX2 optical modules. Data transmitted by the PCI9054 card on the bi-directional control bus (16-bit input plus 16-bit output) are buffered and stored on two 16-bit wide / 4-Mbit depth FIFOs (named “FIFOrx” and “FIFOtx”). The TRX module reads control data from the FIFOtx and sends them to the MBOpt board and vice versa writes on the FIFOrx the control words coming from the MBOpt board. In a similar way, one 32-bit / 4-Mbit depth FIFO memory (named “FIFOrx2”) is provided along the readout path. The RX2 module receive the (readout) data from the MBOpt board and write them into the FIFOrx2. These FIFO memories are used to decouple the optical link stage data/control busses from the PCI9054 ones. In this way the optical setup and the PCI card can run different clocks and phase problems are avoided. And there is not need to transmit clock signal over the cable.
An FPGA-based controller manages the optical modules and the FIFO chips but is not interfaced with the control bus. Operation codes for the OptHub card are sent through the general purpose pin (see below). An I²C communication bus is provided to read the temperature of the optical transceivers (HFBR5912).

Below the main sections of the hardware design will be described.

5.1.1.1 The board controller (fPGA)
The Xilinx’s XC2S150E-TQ144 fPGA is used as board controller. It manages all the control/status signals of the board devices (FIFOs, optical modules, I/O drivers, etc.).
Chapter 3 – The PPC Imaging System: the *OptHub* card

The control logic can be divided in different sections (fig. 19):

- **FIFO tx controller**: the fPGA monitors the status of the FIFOtx through the empty (EF#) and full (FF#) flags and controls both the read and write operations through the FIFOtxREN# and FIFOtxWEN# signals. The FIFOtxWEN# signal is asserted when the PCI9054 sends control word to the OptHub while the FIFOtxREN# is asserted these to send these data to the MBOpt through the optical link. When the system is in idle state, the FIFOtx EF# flag acts as interrupt signalling that new control data have been stored. The FIFOtx can be reset by the FIFOtxMRS# signal;

- **FIFO rx controller**: the fPGA monitors the status of the FIFOrx through the empty (EF#) and full (FF#) flags and enables the data reading asserting the FIFOrx read enable (FIFOxREN#) pin. The FIFOrx write enable pin can be automatically asserted by the TRX module through the DAVRx# signal or by the fPGA (FIFOxWEN#). The FIFOrx can be reset by the FIFOxMRS# signal;

- **FIFO rx2 controller**: the fPGA monitors the empty (FIFOx2EF#) and full (FIFOx2FF#) flags of the FIFOx2 chips and controls both their read operations through the FIFOx2REN#. The FIFOx2 write enable pin can be automatically asserted during the acquisition of readout data directly by the RX2 module through the DAVRx2# signal or by the fPGA (FIFOx2WEN#). The FIFOx2REN# is asserted when the PCI9054 card requests the readout data stored in the FIFOtx2. The FIFOtx2 chips can be reset by the FIFOtx2MRS# signal;

- **TRX module controller**: the fPGA monitors the main status signals from the TRX module (LOCK_TX#, RDY_RX#, SD_RX#, ERR_SD#) to check if the optical module is ready to send and receive data, checks if the MBOpt is sending control data by the status of the DAV_RX, TRG_RX receiver flags, and controls the data transmission operation through the DAV_TX#, TRG_TX signals. The PASSRx# signal can be set when the HDMP-1034A “Parallel Automatic Synchronization System” (PASS) feature is required (see the Optical Link setup paragraph). The TRXPRSNT# signal indicates if the TRX module is connected or not;

- **RX2 module controller**: the fPGA monitors the RDY_RX#, SD_RX#, ERR_RX# flags to check the status of the optical transmission channel and the TRG_RX#,
**Chapter 3 – The PPC Imaging System: the *OptHub* card**

**5.1.1.2 The TRX optical module interface**

The TRX input (DTX[0:15]) and output (QRX[0:15]) data busses are directly connected to the FIFOtx output and to the FIFOrx input whereas the control and control/status signals (TRGRx, RDYRx, ERRRx, SDRx, RSTRx, DAVRx, PASSRx, TRGTX, LOCKTx) are routed to the fPGA. The TRX flag bits are not used. The recovered clock (CLOCKOUTRx) coming from the TRX receiver is first buffered by a clock buffer (IDT’s ICS8302) and then can be used to drive the FIFO rx write clock (FIFORxWCLK) when the local reference clock is not used (“PASS” mode disabled). An hardware switch allows the DAVRx# signal to drive the FIFOtx write enable (FIFOTxWEn#).

The mechanical link is obtained by two slim 100-pin plug connectors (Robinson Nugents’ P08-100PL-A-TG). Three hard-coded pins are used to check the type and the presence of the optical module. Two of them drive two LEDs to indicate the user that the correct module is inserted (both LEDs have to switch-on) while the third pin is routed to the fPGA to signal if the module is actually inserted or not (TRXPrsnt#).

**5.1.1.3 The RX2 optical module interface**

The RX2 output data bus (QRX2[0:31]) is directly connected to the FIFOrx2 input whereas the control and status signals (TRGRx, RDYRx, ERRRx, SDRx, RSTRx, DAVRx, PASSRx) are routed to the fPGA. The RX2 flag bits are not used. An hardware switch allows the DAVRx# signal to drive the FIFO rx2 write enable (FIFORx2WEn#). The recovered clock (CLOCKOUTRx2) is first buffered by a clock buffer (IDT’s ICS8302) and then can be used to drive the FIFO rx2 write clock (FIFORx2WCLK) when the local reference clock is not used (“PASS” mode disabled).
Chapter 3 – The PPC Imaging System: the OptHub card

The mechanical link is obtained by two slim 100-pin plug connectors (Robinson Nugents’ P08-100PL-A-TG). As for the TRX module, two LEDs are used to decode if the right module has been inserted while a third line (rtx2PRSNTH) signals to the fPGA if the module is actually inserted or not.

5.1.1.4 I/O connectors

The Opt-Hub card is in the middle of DAQ interfacing the detector stage with the PCI card. On the PC side the card exploits two 80-pin header connectors (3M’s 81080-6) while on the detector side three MT-RJ connectors are used to connect the optical fibres. One JTAG connector allows to access the program memory of the fPGA and flash PROM.

5.1.1.5 General purpose lines

Beside the data and control lines, each header connector offers other four single-ended (GIO[0:3], GIO[4:7]) and two differential (LVDS[0:1], LVDS[2:3]) signals which can be used as general purpose I/O lines to transmit or receive further signals to/from the PCI9054 card. The two 4-bit general purpose bus can be configured as input or output by a 74LVC244 device configured as 4-bit bi-directional buffer (fig. 20).

![Fig. 0.81. The 4-lineCMOS bi-directional driver circuit.](image)

Two of the differential pairs (one for each connector) can be configured as input or output by the bi-directional LVDS/CMOS transceiver DS90LV019 (fig. 21) while the other twos can be used to send the PCI clock on the OptHub. All this signals (except...
the last two) are routed to the fPGA and in the actual design are used to send control word to the fPGA.

5.1.1.6 I2C controller

One parallel-bus to I2C-bus controller (Philips’ PCA9564APW, 20-pin TSSOP31) is used to drive the I2C temperature sensors on the optical modules. The PCA9564 serves as an interface between most standard parallel-bus and the serial I2C-bus and allows the parallel bus system to communicate bi-directionally with the I2C bus. This controller can operate as a master or a slave and can be a transmitter or receiver. Communication with the I2C bus is carried out on a byte-wise basis using interrupt or polled handshake. The PCA9564 takes care of all the I2C-bus specific sequences, protocol, arbitration and timing with no external timing element required.

Fig. 0.83. The I2C bus interface circuit.

The PCA9564 data (D[0:7]) and control (CE#, WR#, RD#, INT#, RESET#, A[0:1]) signals are directly connected to the fPGA. An external pull-up resistor (10k) is required for the I2C clock (SCL) and I2C data (SDA), and for the interrupt (INT#) lines (fig. 22).

5.1.1.7 Clock generator circuit

The main clock circuit is based on a 40-MHz small-package crystal oscillator (Jauch Quartz’s VX3MH4000) coupled with one clock buffer (Cypress’s CY2309-1H, 16-pin SO32) that fan out the clock signal from the oscillator into up to 9 clock signals with zero delay (<350 ps input-to-output propagation delay) and very low skew (<250 ps output-to-output skew) between the outputs. The clock buffer outputs drive the fPGA (FPGA_CLK), the TRX and RX2 modules (CLK40), the FIFOtx read clock

31 Thin Shrink Small Outline Package.
32 8-pin Small Outline package
(\texttt{FIFO}Tx\texttt{RCLK}), and can drive also the \texttt{FIFORx} write clock (\texttt{FIFO}Rx\texttt{WCLK}) and the \texttt{FIFORx2} write clocks (\texttt{FIFO}Rx2\texttt{WCLK}) if requested (see the previous \texttt{FIFORx} and \texttt{FIFORx2} sections). All the clock traces are can be well terminated by a circuit to match the correct impedance.

### 5.1.2 PCB layout

The PPC \textit{Opt-Hub} card was manufactured by Baselectron factory (Pavia, IT) in 6-layer PCB with the following stack:

1. TOP (routing);
2. PWR (+3.3 V plane layer);
3. GND (plane layer);
4. IN2 (routing, power planlet layer);
5. IN1 (routing, GND planlet);
6. BOT (routing).

![Screenshot of the OptHub layout designed by the OrCAD LAYOUT program.](image-url)
All the active components are positioned on the PCB top side except the I²C bus interface and the header sockets.

The dimensions of the present PCB are 16 cm x 18 cm but a more compact layout is ongoing.

Fig. 0.85. PCC Opt-Hub card top side PCB. The main parts of the board are pointed out for text reference. The PCB dimensions are 16 cm x 18 cm
6 The Motherboard\textsubscript{Opt} card

The Motherboard board supports the detector carrier card (\textit{Chipboard\_4C}) and one of the optical link ends (\textit{TX2} and \textit{TRX} modules). It houses the TX2/TRX optical modules, a 4-Mbit depth FIFO and one fPGA which provides the Medipix2 logical interface and manages the I\textsubscript{2}C bus and the FIFO memory. Readout data coming from the Medipix2 quad are not handled by the FPGA but simply stored in FIFO buffer memory.

The development of this card was splitted in two steps: first, a card without the optical link support (the \textit{Motherboard\_TEST}) has been built directly interfacing the PCI card through flat cables (Fig. 1b); then the board project was modified by adding the optical link modules. This solution simplifies the DAQ system debug and the test procedures on the Chipboard\_4C card.

The fPGA can be programmed by the flash PROM or through the JTAG interface.

6.1 Preliminary design consideration

The Medipix2 parallel readout feature (milestone) have a great impact on acquisition system design. First of all, data transfer over the 32-bit wide bus requests a close interconnection between the Medipix2 and acquisition/storing circuitry. It should be accomplished by short flat cables (see also MaxiPix system in Chapter 2).

The simpler solution to overcome this problem consists of putting the chip directly on the control board. This choice is not much flexible because / has the great disadvantage that …

A more flexible approach consists of put the detector on a different board. The great advantage is that different detectors can be quickly connected to the control board. Moreover, the control and the detector carrier boards can be developed separately and if request upgraded without affecting the other card (when the hardware and signal interface is kept). It is the same paradigm adopted by the MaxiPix and RUIN readout systems (Chapter 2).
Chapter 3 – The PPC Imaging System: the Motherboard\textsubscript{Opt} card

In the PPC system, the motherboard and chip carrier cards are connected together by a couple of slim 100-pin plugs, offering a good mechanical and electrical link and a reduced occupancy on the PCB. The \textit{CB}\textsubscript{4C} is connected on the \textit{MB}\textsubscript{Opt} bottom layer as a mezzanine module with the detector facing the \textit{MB}\textsubscript{Opt} bottom side. Then a 3cm x 3cm window is requested on the \textit{MB}\textsubscript{Opt} PCB to shine the detector. This arrangement allows to attach a heat sink on rear side of the detector and at the same time to protect the Medipix2 micro bonding wire against damages.

![Diagram](image)

Fig. 0.86. Sketch of the PPC system detector stage. The profile view shows the arrangement of the \textit{Chipboard}_4C card and optical modules \textit{TRX} and \textit{TX2}.

### 6.2 The hardware architecture

The \textit{MB}\textsubscript{Opt} acts as control / interface board. It supports the \textit{Chipboard}_4C card and one end of the optical link setup (fig. 20). The half-duplex 16-bit data channel provided by the \textit{TRX} module is connected to the fPGA controller through two 16-bit wide, 4-Mbit depth FIFOs (“FIFO\textsubscript{tx}” and “FIFO\textsubscript{rx}”) to decouple the optical link stage from the detector one. For the same reason, one 32-bit / 4-Mbit depth FIFO memory (“FIFO\textsubscript{tx2}”) is provided along the readout path.
Fig. 0.87. Block diagram of the PPC Motherboard_{opt} card.

The fPGA also manages the control and status signals of the FIFO memories and drives the Chipboard_{4C} interface but cannot handle the readout data.

The system clock is fixed and its value is 40 MHz. All the active chips are synchronous with the system clock. Dedicated power supply circuit are provided for the optical link modules and for the Chipboard_{4C}.

The main sections of the hardware project are described below.

6.2.1.1 The fPGA master board controller

The MB_{opt} is managed by a master controller implemented on a fPGA (Xilinx’s Spartan-II E XC2S200E, TQ208). The master controller logic is implement in a fPGA (Xilinx’s). This device accepts input data and command codes from the 16-bit output port of the TRX module, and can output data by the 16-bit input bus of the same optical module.

The control logic can be divided in different sections, that is:

- **FIFO{rx} controller**: the fPGA monitors the status of the FIFO{rx} through the empty (EF#) and full (FF#) flags and enables the data reading asserting the FIFO read enable (FIFO{rx}REN#) pin. When the system is idle, the EF# flag acts as interrupt signalling a new operation code. The FIFOx can be reset by the FIFO{rx}MRS# signal;

- **FIFO{tx} controller**: the fPGA monitors the status of the FIFO{tx} through the empty (EF#) and full (FF#) flags and controls both the read and write operations...
through \texttt{FIFOtxRen} and \texttt{FIFOtxWen} signals. FIFOtx can be reset by the \texttt{FIFOtxMRS} signal;

- **FIFOtx2 controller**: the fPGA monitors the empty (\texttt{FIFOtx2Eff}) and full (\texttt{FIFOtx2Eff}) flags the FIFOtx2 chips and controls both the read and write operations through \texttt{FIFOtx2Ren} and \texttt{FIFOtx2Wen} signals. The \texttt{FIFOtx2Wen} signal is asserted during the readout operation while the \texttt{FIFOtx2Ren} is asserted to transmit the readout data to the \textit{Opt-Hub} card. The FIFOtx2 chips can be reset by the \texttt{FIFOtx2MRS} signal;

- **TRX module controller**: the fPGA monitors the main status signals from the TRX module (\texttt{Lock-tx#}, \texttt{RDY-rx#}, \texttt{SD-rx#}, \texttt{ERR SD#}) to check if the optical receiver is properly working and controls the data transmission operation through the \texttt{DAV tx#} signal;

- **TX2 module controller**: the fPGA monitors the \texttt{Lock-tx2#} flags to check the status of the optical transmission channel and controls the data transmission through the \texttt{DAV tx2#} lines during the readout operation;

- **CB_{4C} interface controller**: the fPGA manages the I/O serial data lines (\texttt{CB sdi}, \texttt{CB sdo}), the address (\texttt{CB ad}), control (\texttt{CB ctrl}, \texttt{CB rst}, \texttt{CB en}) and status (\texttt{CB busy#}, \texttt{CB dav#}) lines of the \textit{Chipboard 4C} interface. A 16-bit parallel-to-serial register and serial-to parallel registers are used to send/receive data to/from the CB_{4C} through the serial data channel. The address bit are set one of four Medipix2 chips of the quad. The 4-bit \texttt{CB ctrl} line are used to set the operation code while the \texttt{CB en} and \texttt{CB rst} lines needs to start the selected operation and reset the CB_{4C} board, respectively. Status flags are used to check if some peration is ongoing is (\texttt{CB busy#}) and if the operation has been properly accomplished (\texttt{CB dav#}) or not;

- **I\textsuperscript{2}C bus controller**: the fPGA accesses the \textsuperscript{2}C bus through the PCA9564 interface which requires to control the 8-bit data bus (\texttt{I2c d[0:7]}), the address (\texttt{I2c a[0:1]}), control (\texttt{I2c wr#}, \texttt{I2c rd#}, \texttt{I2c cs#}, \texttt{I2c rst#}) and the interrupt (\texttt{I2c int#}) lines (see also the \textquotedblleft \textsuperscript{2}C interface\textquotedblright{} section below).
Chapter 3 – The PPC Imaging System: the *Motherboard* card

**Control logic block**: the fPGA supervises all the board resources and operations by the control logic block (CLB). The CLB is implemented as a Mealy’s finite-state machine (FSM) which controls the logic state of all the signal depending on its state and its input. All the fPGA logic blocks are managed by the CLB. A description of the FSM working mode can be found further on in the “Communication protocol” paragraph.

The fPGA is interfaced with a flash PROM (Xilinx’s XCF04S, 20-pin VO20) which stores the configuration file or “bit stream”. The configuration interface consists only on a serial data line (DIN), a clock line (CCLK), and two control lines (INIT# and DONE). Moreover the fPGA can be programmed on-fly by the 4-wire JTAG standard interface (TDI, TDO, TMS, TCK).

Upon power-up or reconfiguration (the fPGA PROGRAM# pin is asserted), the fPGA automatically loads the configuration bit stream from the external PROM synchronized by the configuration clock (CCLK) generated by the fPGA itself (“Master Serial” configuration mode33). Data from the PROM are read out sequentially on a single data line (DIN), accessed via the PROM’s internal address counter which is incremented on every valid rising edge of CCLK.

---

33 The fPGA's mode select pins (M0 to M2) are used to select the configuration mode.
At start up (or when the fPGA program\# pin is tied down) the fPGA generates a configuration clock (cclk) that drives the PROM and loads the configuration bit stream from the PROM (“Master Serial” configuration mode).

All the programmable logic of the detector stage (fPGA, PROM, and the chipboard’s CPLD) are daisy-chained and are programmable through the JTAG board connector. When the CB\textsubscript{4C} is not connected to the MB\textsubscript{Opt} the daisy chain is shorted by an hardware switch.

Fig. 0.89. Block diagram of the serial configuration chain (“Master Serial” mode).

All designs for the Xilinx FPGA’s are done in the Verilog Hardware Description Language (HDL) utilizing Xilinx’s Foundation series software.

6.2.1.2 Voltage Level Translator

The Medipix2 readout bus is 2.2 V LVCMOS compliance. In order to match the with the minimum input “logic 1” level of the FIFO chip (2.0 V) two 16-bit voltage level translators (74ALVC164245, 48-pin SO) are foreseen. These chip are programmed to translate the 2.2 V bus into a 3.3 V bus.
Chapter 3 – The PPC Imaging System: the *Motherboard* card

Fig. 0.90. Screenshots form the voltage level translator circuit. The bit0 of the parallel bus is captured during a parallel readout operation before and after the voltage level translator chip. Signal amplitude rises up from ~2 V to ~3.3 V (left figure). The overshoot remain stable (40 %) while the propagation delay is about 4 ms (compatible with AC characteristics).

### 6.2.1.3 FIFO memory buffers

Several FIFOs (IDT’s 72V2113L10) are provided to decouple the data bus of the detector stage from the one of the Opt-Hub. The 32-bit readout channel needs two FIFOs (“FIFOTx2”) connected in pair\(^{34}\) to increase the word width. Data coming from the Medipix2 parallel bus card are stored into the FIFOTx2 before to be sent to the *Opt-Hub* by the TX2 module.

Fig. 0.91. Screenshot showing the FIFO input data (bit0) and the write clock. Setup time is about 5 ns and the hold time is about 20 ns. It matches the FIFO minimum ratings.

---

\(^{34}\) The read/write enable control signal and the reset pins of the two chips are tied together while the empty/full flags are independent.
Other two FIFO are provided as TRX module data buffer, one for the receiver (“FIFO\textsubscript{rx}”) section and the other for the transmitter (“FIFO\textsubscript{tx}”) one. Data coming from the Opt-Hub card (via the optical link) are stored by the TRX on the FIFO\textsubscript{rx} before to be processed by the fPGA. Vice versa data to be transmitted toward the Opt-Hub are first stored into the FIFO\textsubscript{tx} and then are read by the TRX.

6.2.1.4 \textbf{I}^2\textbf{C} bus controller

The Philips’ PCA9564APW is used to drive the I\textsuperscript{2}C bus (see also paragraph 10.2). It allows the fPGA to communicate bi-directionally with the I\textsuperscript{2}C chips on the CB\textsubscript{4C} card (DAC, ADC and Medipix2 temperature sensor) and on the TRX/TX2 (temperature sensor on the optical transceiver).

The PCA9564 data (D[0:7]) and control (CE\#, WR\#, RD\#, INT\#, RESET\#, A[0:1]) signals are driven by the fPGA. External pull-up resistors (10k) are required for the I\textsuperscript{2}C clock (SCL) and data (SDA), and for the interrupt (INT\#) lines.

6.2.1.5 \textbf{Power supply circuit}

The MB\textsubscript{opt} supply circuitry is divided in three different sections:

- “Board supply circuit” is powered from a single 5 Volt / 1A DC power source. The following local DC voltages are required: +3.3 V, +1.8 V (fPGA), +2.2 V (voltage level translator). These voltages are derived from the 5 V DC power source by three DC/DC converter modules located on the bottom side of the PCB.
- “Chipboard supply circuit” is powered from a 5 Volt / 2A DC power source to derive the following local DC voltages: +2.2 \textsubscript{V\textsubscript{DISP}}, +2.2 \textsubscript{V\textsubscript{ANA}}, +3.3 V, +1.8 V.
- “Optical modules supply circuit” is powered from a 5 Volt / 2A DC power source and provided two DC voltage lines: +3.3 V (adj) for the HDMP-1032A serializers (TX2 and transmitter section of the TRX) and +3.3 V (adj) for the HDMP-1034A deserializer (transmitter section of the TRX module). Both supplies are obtained by two 3 A adjustable linear regulators (LM1086IS-adj, TO263) in order to trim the best voltage supply for each section (see paragraph 3.xx).
Fig. 0.92 Picture of the optical link section on the Motherboard_{opt} card.
7 The “Chipboard_4C” card

The most demanding component of the PPC system is the chip carrier board named *Chipboard_4C* (below referred as CB). It was designed to hold the hybrid x-ray detector based on the Medipix2 quad ASIC. Special effort on this design derives from the use of the Medipix2 parallel bus as readout channel. It implies that 32 pad must to be foreseen on 32 PCB for the wire bonding and that 32 copper tracks have to be routed on the PCB. Moreover the quad assembly houses four chips which further complicate the footprint design.

### 7.1 Preliminary design considerations

The Medipix2 quad interface requires a high-density displacement of pad for the wire bonding connection. These pad must be large enough (~ 100 μm) to allow a reliable bonding\(^{35}\). When the parallel bus is needed, quite all the I/O pads have to be connected and the only solution is to make a PCB with linear array of small pads facing the Medipix2 I/O pads in a one-to-one fashion (fig. 19).

![Medipix2 I/O pads layout](image)

**Fig. 0.93.** Sketch of the layout interface between the Medipix2 chip periphery and the *Chipboard_4C* PCB.

\(^{35}\) Usually thin wires (about 20 micron in diameter) are used for the wire bonding and the bond width on the pad is usually 1.5÷2 times the wire diameter. Moreover the tolerance on the micro solder machine positioning should be taken into account.
The Medipix2 I/O pads have a 120 μm pitch with a 108 μm width. Commercial available PCB allows for about 50 μm tracks with 50 μm spacing footprints. The straight solution would consist on an array of 70 μm wide pads spaced by with 70 μm but in order to further increase the pad width, a staggered footprint was adopted to maximize the bonding pads width up to 90 μm (fig. 20).

Fig. 0.94. Staggered design of the bonding pads on the Chipboard_4C PCB.

Such a challenging layout was commissioned to an external qualified factory (Zener s.r.l., Pozzuli (Na), Italy) skilled on high density PCBs. Instead, the schematic project is developed in the behalf of this thesis work.

Fig ? shows the top and bottom side silk-screen printing of the final CB4C PCB. Outside dimensions are 8.3 cm x 9.5 cm.
Chapter 3 – The PPC Imaging System: the Chipboard_4C card
Fig. 0.95. Silk-screen printing of top (up) and bottom (down) layers of the $CB^{4C}$ PCB (dimensions are in mm).

Fig. 0.96. Detail of footprint corresponding to the lower left corner of one Medipix2 chip.

The link with the Motherboard card is obtained by two slow-profile high-density 100-pin connectors (Robinson Nugent’s, P08-100SLA-TG). About one half of the
contacts are grounded and most of the remaining ones are for the parallel bus and power supply. In order to limit the number of interface signal, a complex programmable logic device (CPLD) manages all the configuration, data and clock signals of the four chips. Moreover, one 4-ch 10-bit DAC provides a variable voltage (DAC\_IN) to each Medipix2 chip whilst one 4-ch 12-bit ADC can read the analogue reference settings of the chips (DAC\_OUT); both ADC and DAC have the I\textsubscript{2}C standard interface. A voltage reference circuit is implemented for the Medipix2 internal DAC bias, while five 4-ch LVDS-to-CMOS transceivers provide the right signalling conversion for the clock, enable and data lines of each chip.

8.1. Hardware architecture of the PPC Chipboard\_4C card

The CB4C card contains the front-end circuitry for the Medipix2 quad chip. It must drive the enable, data, clock and operation mode signals of four Medipix2 chips.

Even if the Medipix2 pads layout is suited for daisy-chain connection between adjacent chips, such a solution does not fit with the PPC design because of the propagation delay (about 7 ns) introduced on the clock signal by each chip of the chain. It means that the fourth chip receives a clock with a phase delay of about 24 ns, which is quite less than the system clock period (25 ns at 40 MHz). It is a critical issue during the parallel readout because it would request the use of the Medipix2 output clock (FCLOCK\_OUT) to synchronize the Motherboard readout data FIFOs. In order to save pins and reduce the routing complexity, the Medipix2 output clock is not implemented and all operations are synchronous with the system clock (CLK). So four independent clock (CLOCK\_IN), data (DATA\_IN) and enable (ENABLE\_IN) signals are provided to each chip and four data (DATA\_OUT) and enable (ENABLE\_OUT) signals are read from quad. All these signals are driven by the CMOS-to-LVDS tranceivers placed between the CPLD and the Medipix2 chips. Instead control (RESET, SHUTTER), operation mode (M0, M1), acquisition (POLARITY, P\_S), (POLARITY, P\_S) signals are directly driven by the CPLD and are common for all four chips.
Chapter 3 – The PPC Imaging System: the Chipboard_4C card

The interface with the motherboard control card

7.1.1.1 The Medipix2 quad interface
The chip carrier board was specifically developed to house one x-ray hybrid detector based on the Medipix2 quad with the parallel readout mode feature.

The presence of four Medipix2 chips and the parallel readout implementation mode have implied several design constraints. In order to avoid the routing of a 32-bit bus across the PCB, the readout bus is shared between each couple of adjacent chips and is routed to nearest connector. The drawback is that chips have to be read sequentially as they were in daisy-chain.

A large heat sink area is provided to conduct heat away from the Medipix2 quad.

7.1.1.2 The I/O interface
The CB_4C signal interface is similar to that of a standard multichannel IC (like DAC or ADC): beside the clock (CLK), the address bus (AD[0:2]) is used to select one of the four chips (of the multisector detector), the control bus (CTRL[0:3]) is used to set the operation code, the serial input (SDI) and output (SDO) data lines are used for write and read accesses, and finally a board reset (RST#) and one enable operation (EN#) pins are provided. A JTAG access port is present to configure the CPLD. Two output flags are foreseen to signal if any ongoing operation (BUSY#) and to signal some fault
condition (DAV#). These two bits can be reprogrammed as needed to accomplish other different functions.

The CB4C is connected to the Motherboard card by two slow-profile high-density 100-pin connectors (Robinson Nugent’s, P08-100SLA-TG). Contact are displaced on two rows. The first and last 8 contact of each connector are reserved to the power supply lines (2.2 V digital, 2.2 V analog, 3.3 V, 1.8 V). Other 32 bit of each connector are dedicated to the parallel bus. Data lines are interleaved with ground pins to reduce crosstalk effects. The remaining pins are used for the control code.

7.1.1.3 The Complex PLD chip

A CPLD chip is used as main controller of the board. It provides a flexible interface between the signal interface with the MotherboardOpr card and the Medipix2 quad chip.

Its function can be divided in different logic block as follows:

- **Clock in Demultiplexer**: the system clock (CLK) is routed to one of the four CPLD clock output pin (FCLOCK_IN[0:3]) depending on the status of the address lines (AD[0:2]). When the “matrix reset” operation is performed, it is possible to activate all the clock lines at the same time.

- **Data in Demultiplexer**: the serial data stream (CB_SDI) coming from the MotherboardOpr FPGA is routed to one of the four CPLD data output (DATA_IN[0:3]), depending on the status of the address lines (AD[0:2]), or to the internal configuration register. For test purpose, when no operation is running, the serial data input (CB_SDI) is directly routed to the serial output (CB_SDO).

- **Enable in Demultiplexer**: the enable signal (CB_EN) coming from the MotherboardOpr FPGA is sent to one of the four chips data input (ENABLE_IN[0:3]) depending on the status of the address lines (AD[0:2]). When the “matrix reset” operation is performed, it is possible to enable all the chips at the same time.

- **Data out Multiplexer**: the serial data output lines (DATA_OUT[0:3]) coming from the Medipix2 chips are routed to the chipboard serial output (CB_SDO). The status of the address lines (AD[0:2]) set the multiplexer.
- **Enable out multiplexer**: the enable data output lines (ENABLE_OUT[0:3]) coming from the Medipix2 chips are routed to the chipboard serial output (CB_SDO). The status of the address lines (AD[0:2]) set the multiplexer.

- **Operation Mode LUT**: the status of the output lines reset, shutter, m0, m1 is stored on a look-up table and is selected by the CTRL[0:3] lines.

- **Configuration register**: when “idle” code is set on the CTRL lines and the chip is enabled (CB_EN goes high) the serial input data are routed in a 16-bit shift register which after 16 clock cycles stores its content in the configuration register. The status of POLARITY, P_S, SPARE_FSR[0:3], EN_TPULSE[0:3] signal is mapped on this configuration register.

Several output test pads and LEDs are available for test purpose.

### 7.1.1.4 The LVDS/CMOS drivers

As the Medipix2 clock/data/enable signal are LVDS type, five LVDS/CMOS drivers are used to match the CPLD CMOS signals with the LVDS standard. Three CMOS-to-LVDS signal translators (National Semiconductor’s DS90LV047A, 16-pin SO) are used to drive the FCLOCK_IN[0:3], DATA_IN[0:3], ENABLE_IN[0:3], while two quad LVDS-to-CMOS (DS90LV048A) are used for the DATA_OUT[0:3], ENABLE_OUT[0:3] differential signals coming from the Medipix2 chips. The DS90LV047A/048A are quad CMOS flow-through differential line driver designed for applications requiring ultra low power dissipation and high data rates (up to 400 Mbps) utilizing Low Voltage Differential Signaling (LVDS) technology. The DS90LV047A accepts low voltage TTL/CMOS input levels and translates them to low voltage (350 mV) differential output signals. Vive versa the DS90LV048A accepts low voltage (350 mV typical) differential input signals and translates them to 3V CMOS output levels.

### 7.1.1.5 Voltage Reference circuit

A simple shunt voltage reference circuit based on the (National Semiconductors’ LM4041CIM3-ADJ, 5-pin SOT-23) provides the bias voltage (1.324 V) for the Medipix2 internal DACs (DAC_BIAS). The voltage reference output can be adjusted within 1 mV by a multi-turn trimming potentiometer used as feedback resistor. When the Medipix2 MXR is used this reference circuit can be bypassed by the chip internal reference.
7.1.1.6 The Analog-to-Digital converter

One 4-ch 12-bit DAC (Analog Devices’ AD5325BRM, 10-pin MSOP\textsuperscript{36}) is foreseen. It could be programmed by the I\textsuperscript{2}C bus (SCL, SDA) to replace one of the Medipix2 internal DACs when more precision is required (12-bit instead of 8 bit) or in case of damage. The references for the four DACs is derived from one high precision voltage reference chip (National Semiconductors’ LM4140-2.0, 8-pin SO) which provides a low drift and noise 2.048 V reference.

The AD5325 is controlled via an I\textsuperscript{2}C compatible serial bus. The DACs are connected to this bus as slave devices. The AD5325 has a 7-bit slave address. The 6 MSB are 000110 and the LSB is determined by the state of the A0 pin (up to two of these devices can be connected on one bus).

\textbf{Fig. 0.98.} Internal block of the AD5325 DAC chip.

\textsuperscript{36} Mini Small Outline Package.
7.1.1.7 The Digital-to-Analog chip

One 4-channel 10-bit ADC (Analog Devices’ AD7417BRM, 16-pin SOIC\textsuperscript{37}) is used to read the voltage setting of the Medipix1 internal DAC. Each analog input channel (A\textsubscript{IN}[1:4]) is connected to the DAC\textsubscript{OUT} pin coming from one different Medipix2 chip. Control of the AD7417 is carried out via the I\textsuperscript{2}C compatible serial bus (scl, sda). The AD7417 is connected to this bus as a slave device, under the control of the PCA95xx master device (see Motherboard\textsubscript{OPT} card). A conversion is initiated every time a read or write operation takes place through the I\textsuperscript{2}C bus (automatic conversion mode). The AD7417 embeds also one temperature sensor that is useful to monitor the quad working temperature. An over temperature interrupt (oti) is foreseen to signal

The ref\textsubscript{IN} input is tied to ground to enable the on-chip 2.5 V reference.

As with all I\textsuperscript{2}C compatible devices, the AD7417 have a 7-bit serial address. The four MSBs of this address are set to 0101, while the three LSBs can be set by connecting the A\textsubscript{2} to A\textsubscript{0} pins to either VDD or GND. The address can be configured by an array of resistors.

Fig. 0.99. Internal block diagram of the AD7417.

\textsuperscript{37} Small Outline Integrate Circuit.
Fig. 0.100. The ADC circuitry based on the AD7417.

Fig. 0.101. The screenshot shows the Medipix2 parallel bus bit0 (upper trace) and the readout clock (FCLOCK_IN) at the input of CMOS-to-LVDS converter. The data-to-clock delay for a low-to-high transition is about 8 ns.
7.2 Summary

In this chapter a detailed description of the PPC readout system has been presented. All the system is based on custom designed electronic boards. Due the complexity of the design was split in two steps in order to simplify the development and the debug operations. In first step a simplified “test setup” based on a cable interconnect between the detector stage and host PC was developed. The actual version of this test setup represents a complete readout system for the Medipix2 quad. In a following step, the setup was upgraded with the optical link interconnect. This step has required the develop of the OptHub card and the upgraded version of the motherboard card. The system is tested as described in the Chapter 4.

Based on the actual design several improvements are foreseen as follows.

The Motherboard can be upgraded by using an FPGA between the parallel bus output and the FIFO buffer. It could be work as voltage level translator and at the same time could handle output data to perform de-serialization and decrypt. Moreover it could be programmed to “simulate” the Medipix2 detector allowing the test of DAQ system without the chipboard card. A preliminary study as shown that such a design would request a BGA package FPGA. This is the way this design was not implemented for the first release of the PPC system.

The use of the decoupling FIFOs allows to use a different clock for the chipboard card. This clock could be adjusted to achieve the best readout performance.

The OptHub card layout can be optimised halving the PCB dimensions. Preliminary design and layout draft are already available.

The interface with the host PC may be upgraded in two different way: First, improving the PCI9054 card to hold the optical link transceivers (by a mezzanine card or directly on the PCI card itself); second, exploiting the faster PCleexpress bus\textsuperscript{38} by a new and different interface card.

\textsuperscript{38} The slower PCleexpress interface (1x) has a nominal bandwidth of 266 MB/s, which doubles the PCI 32-bit/33-MHz data rate.
7.2.1 Bibliography


[Fan06] Fanti V., Marzeddu R., Randaccio P., “PCI card with DMA capabilities for digital imaging detectors readout”,


[PCI2.2] PCI Special Interest Group, “PCI Local Bus Specifications rev. 2.2”, Dec. 1998

Chapter 4:

Characterization of the PPC Imaging System

Abstract - The PPC imaging system has been realized as described in the previous chapter. It consists of different custom-designed electronic cards and exploits an hybrid photon-counting detector - based on the Medipix2 quad readout ASIC – with an active area of about 3 cm x 3 cm. Programmable logic chips are used to model the low-level protocol of the electronic boards while the whole system is controlled through a Graphical User Interface (GUI) running on the host PC.

This chapter aims to explain how the PPC imaging system works. The communication protocol of the hardware, the firmware of the programmable logic devices and the GUI developed to manage the acquisition system will be described. Obtained results and status of development of the PPC system will be outlined.

Test image acquired by the PPC imaging system (parallel readout mode). The image is obtained shining a copper wire put on the detector surface by means a $^{90}\text{Sr}$ source (100 Ci).
8 Characterization of the PPC system

As conclusive part of the work, the hardware of the PPC system (see Chapter 3) has been tested and characterized. The acquisition chain is controlled by a host PC running Microsoft® Windows XP professional. The PC (IBM S50) is equipped with a 2 GHz PentiumIV® processor and 4 GB of DDR RAM. Two PCI slot (32-bit / 33 MHz, 5V) are available.

Below the control software application is illustrated. After that, the communication protocols at high (software) and low (firmware) level are described. At the same time, screenshots obtained with a Tektronix TDA3500B oscilloscope are reported to illustrate the characterization tests of the hardware.

8.1 The software application

A control software was developed to manage the imaging system and the Medipix2-based x-ray detector.

The software application is based on a three-tier layered design (fig. 4.1):

- the Graphical User Interface (GUI), which provides a mouse driven interface to communicate with the driver manager;
- the Driver Manager, which provides the connection between the GUI and the lower level driver. It consists of a C-language DLL which receives commands from the GUI and generates Windows API calls to the device driver. Driver manager also allocates and retains data buffers in the user space;
- the Device Driver, which is a Kernel Mode device driver that follows the standard Windows Development Model\(^{39}\) (WDM) to interact with the hardware (i.e. the PCI9054 bridge).

\(^{39}\) The Windows Driver Model (WDM) is a specification for developing device drivers for Windows 98, Windows 2000, and future Windows operating systems.
8.2 The Graphical User Interface

A Graphical User Interface (GUI) referred as *PPCsoft* has been developed together with the hardware of the PPC system. The aim of this software application is to control and test the electronic boards and their low-level communication protocol. Actually the *PPCsoft* should be considered as debug instrument of the PPC system instead of a complete image elaboration software like the MediSoft4 or PixelMan ones.

The GUI has been developed in Visual Basic 6.0 (VB6) for a Windows host environment. It runs on Microsoft Windows98SE, WindowsXP operative systems. VB6 is an event-driven language which allow a fast develop of window-based programs. It is also an interpreted programming language that is very helpful for debug and code development.

8.2.1 The PCI9054 board control panel

The basic function of the *PPCsoft* user application is to connect and use the PCI API DLL (*Device Manager*) to control the PCI9054 card. All the system control is based on the capability to send and receive data through the PCI interface card.

The starting window of the *PPCsoft* is the control panel of the PCI9054 card. (fig. 4.2). It allows to configure and modify the settings of the PLX bridge device, and to test the data communication.
The button “SCAN” starts the scanning of the PCI bus searching for PLX’s devices. If PLX PCI resources are found they are listed in the near listbox from which the user can select one of available devices. After that, when pressing the button “OPEN”, the selected device is opened that is an handle is assigned to that board and then the user can communicate with it (i.e., can perform write and read operations on the PCI board local bus).

All the main parameter relative to the board (such as device type, PCI slot and bus numbers, serial code, memory resources, etc.) are listed on the “device properties” frame on the right of the panel.

On the middle central part of the window the memory spaces allocated by the operative system for the PCI card are summarized by their base addresses and dimensions (or range).
On the bottom part of the window, the “I/O” frame allows a fast test of the read/write operations on the 16-bit bi-directional control (CTRL READ and CTRL WRITE buttons) and 32-bit input data busses (DATA READ button) as reported in chapter 3 (§ 2.xxxx). The PCIWRITE and PCIREAD subroutine are called to accomplish these functions.

Several drop-down menus are available to edit the PCI9054 register set that consists of the PCI Configuration and Local Configuration registers, the EEPROM Configuration register and the DMA group registers. Each of the PCI 9054’s register groups has a distinct dialog box that shows the register values, the register’s PCI base addresses, and a description of the register. Some registers have check boxes and radio buttons to help in describing and setting the register values. Additional dialog boxes are available for more complex registers when required.

8.2.1.1 PCI Configuration Register Group Dialog Box
The PCI Configuration register dialog box (fig. 4.3) allows to set the main parameter of the PCI interface of the PCI9054 bridge.

![PCI Configuration Register Group Dialog Box](image)

Fig. 0.104. The control panel of the PCI9054 PCI configuration register.
The PCI Vendor, Device, Revision, and Class ID codes can be set here together with the size of the. These parameters help the software to distinguish between different boards or systems. Grayed text box indicates read-only values. The radio buttons and check boxes indicate the current settings of the register bit fields. The contents of the dialog box is updated pushing the Refresh button.

8.2.1.2 Local Configuration Register Group Dialog Box
The Local Configuration register values are set through the edit and dialog boxes shown in fig. 4.4. The “range” text boxes reflect the value (in bytes) of the associated register. The memory size is calculated from corresponding register values and cannot be modified directly. To change the memory size it needs to modify the associated register from the PCI Configuration Register panel. Seven registers within the Local Configuration Register Group have a more detailed dialog boxes.

![Local Configuration Registers](image.png)

Fig. 0.105. The control panel of the PCI9054 Local Configuration Register.

8.2.1.3 DMA Register Group Dialog Box
The DMA Register Group dialog box contains the current values for the DMA registers for both DMA channels (see fig. 4.5). The START and ABORT TRANSFER buttons
initiate and terminate the DMA transfer using the current information provided in
the DMA registers for the given DMA channel. The \texttt{CHANNEL ENABLE} bit enables
DMA transfers and activates the Start, Abort, and Clear Interrupt buttons.

This panel allows to test the DMA data transfer to and from the PCI9054 board.

Fig. 0.106. The DMA registers dialog box. It can be used to test the DMA transfer.

Fig. 0.107. Detailed control boxes within the DMA registers block. The DMA Channel 0 settings panel
(left) and descriptor pointers (right) are shown.
8.2.1.4 The EEPROM control panel

The PCI9054 card holds an EEPROM to store the default configuration values for the PCI9054 bridge. The EEPROM control panel (fig 4.7) allows to modify all the fields and load the configuration on the EEPROM.

![EEPROM control panel](image)

Fig. 0.108. The PCI9054 EEPROM control panel.

8.2.2 The Medipix2 control panel

The second fundamental function of the PPCsoft program is to control the PPC system and Medipix2 chip. A global control panel has been designed as shown in fig 4.8 to accomplish all the requested procedures.

Each one of the Medipix2 quas chips can be controlled independently. For each chip is possible to set and read the internal DACs, set and test the active FSR (only Medipix2 chip), set the matrix pixel configuration register, perform the serial and parallel readout.

The acquisition (START COUNTING button) and reset (CHIP RESET button) operation are always performed on all the chips. A global readout button is available to perform the image acquisition from the quad. The readout mode, the charge polarity and the
test pulse switch are set through the setting drop-down menu. Images can be saved in binary and ASCII format through the file drop-down menu.

The global reset board button reset the detector stage (i.e., the motherboard and chipboard cards)

Fig. 0.109. The main Medipix2 MXR test panel. A noise image is shown.

At present the most important Medipix2 operations are implemented as described in the following.

8.2.2.1 “Chip reset”

The simpliest operation is the “chip reset” that performs a general reset of the chip. All counter and configuration (DACs and PCRs) are set to default values. The chip reset is performed by clicking on the “chip reset” button on the Medipix2 control panel. It is a global procedure which acts on all the four chips at the same time.
When the reset button is pressed, the GUI call the `resetChip(address as byte)` subroutine which send the `RESETCHIP` command code to the `MotherboardOn` card. The command code is decoded and forwarded to the `Chipboard4C` to tie down the `MDPX2` quad reset pins. The length of the reset pulse is set by the motherboard fPGA firmware.

![Fig. 0.110. The Mdpx2 CB_RST# and CB_EN# signals during the chip reset operation. The low pulse takes 275 ns (11 clocks).](image)

When the chip reset operation is carried out on the `MDPX2MXR20` chip, the procedure takes care to read back of the identifier code of the four chips (see Ch. 2, § 4.x.x). The quad under test is made of the following chips: chip#0 K9, I8, C10 E9 wafer 48

**8.2.2.2 “DACs setting”**

Another important operation is the “DACs setting” one which allows to tune the `MDPX2` for a correct working. This operation requires to load on the `MDPX2 FSR` the 256-bit configuration string, made of a coded sequence of the DACs configuration values.
DACs values are set by a dedicated window panel (fig. 4.10) which also allows also to save a configuration or load an old one. The change on one single DAC value requires to send the complete configuration string. Slight different panel are showed depending on the actual readout chip (MDPX2 or MDPX2MXR20). If needed, a simpler DAC control panel for a single chip can be visualized (fig 4.11).
When the user press the “SEND CONFIGURATION” button the subroutine “setDACs” 
\begin{verbatim}
(setDacs(chipID as byte, conf () as Integer))
\end{verbatim}
runs. First the configuration string is generated starting by the values provided for each DAC. The configuration string is then divided in sixteen 16-bit word. Finally the setDAC operation code followed by the configuration words are sent in sequence to the motherboard card.

8.2.2.3 “Matrix setting”

The matrix setting operation sets the Pixel Configuration Register (PCR) of the whole chip matrix (see Chapter 1). This operation requires a 917504-bit string made of a coded sequence of the 64k pixels 8-bit configuration values. The change on one single pixel configuration requires to send the complete configuration string. Pixel PCR values are set by a dedicated winwow panel (fig. 4.12) which allows to save a configuration or load an old one.
When the user press the “Configure” button the subroutine “setMatrix()” runs. First the configuration string is generated by the subroutine setMatrixString(byVal chipID as byte, conf () as Integer) which arranges the value of the pixel PCRs in the correct sequence. After that, the string is divided in 57344 16-bit word by the setMatrix16bit(conf () as integer, word () as integer) subroutine. Finally the setMatrix operation code and the configuration words are sent in sequence to the motherboard card.

8.2.2.4 “Serial readout”
This procedure accomplishes the acquisition of the recorded image through the serial readout mode. When the user press the “SERIAL READOUT” button the subroutine “serReadout()” runs. First the serial readout (SRD) operation code is sent to the motherboard. Data are readout, sent to the OptHub and stored in its FIFO_rx memory. After that, the readFifoRx() operation code is sent to the OptHub. A loop of PCIRead() operations (on Local Space 0) generates the read clock and acquire the readout data (serData).
The serial readout data the subroutine \texttt{s\_ deser(IDchip as integer, serData() as long, pseudoCounts() as long)} subroutine reconstruct the pixel counter content (pseudo-counts) and after that the subroutine \texttt{decript(IDchip as integer, pseudoCounts() as long, counts() as long)} gives the real counts of the pixel’s matrix.

Counts are converted in gray level and displayed by the \texttt{display(IDchip as integer, counts() as long)} procedure.

![Image of a fuse taken with the serial readout mode.](image)

The fig.4.13 shows the image of a fuse put on the Medipix2 surface and shined by an uncollimated $^{90}\text{Sr}$ source (100 µCi activity) at a distance of 5 cm from the detector. The detector bias voltage was 70 kV and the acquisition time was 5 s.
Fig. 0.115. Screenshot showing the enable and the FifoRxRen# read enable. The total acquisition time is 60 ms. The first 23 ms are for the serial readout while the remaining 37 ms are for the data acquisition.

The readout phase takes 23 ms, while the acquisition phase takes 1.5 ms for the Motherboard to OptHub data transfer, plus ~37 ms (or ~2.6 ms with DMA acquisition) to move the data on the PC memory (fig. 4.14).

8.2.2.5 “Parallel readout”

This procedure accomplishes the readout of image data through the MDPX2 output parallel bus. When the user press the “PARALLEL READOUT” button the subroutine “parReadout()” (parReadout(chipID as byte, parData() as Long)) runs. First the parallel readout operation code (PRD) is sent to the motherboard. Data are readout, sent to OptHub and stored in its FIFOrx2 (see the Low-level protocols section below). After that, the readFifoRx2() operation code is sent to the OptHub. A PCIRead() operations (on Local Space 1) generates the read clock and acquire the readout data (parData).

From the parallel readout data the subroutine p_deser(IDchip as integer, parData() as long, pseudoCounts() as long) subroutine reconstructes the pixel counter content (pseudo-counts) and after that the subroutine decript(IDchip as integer, pseudoCounts() as long, counts() as long) gives the real counts of the
pixel’s matrix. Counts are converted in gray level and displayed by the
\texttt{display(IDchip as integer, counts() as long)} procedure.

Fig. 0.116. Picture of a fuse acquired through the parallel readout mode (to be compared with fig. 4.13).

The Fig. 4.15 shows the image of a the same fuse of fig. 4.13 taken with the same setup but exploiting the parallel bus. The readout time is \(~4 \times 0.7\) ms, while the acquisition time is \(~4 \times 0.7\) for the \textit{Motherboard}\textsubscript{Opt} to \textit{OptHub} data transfer, plus \(~30\) ms (or \(~1.3\) ms with DMA acquisition) to move the data on the PC memory (fig. 4.16).
The parallel readout picture of fig. 4.15 shows some blind super-columns. These defects are not present in the same image but acquired through the serial readout mode (fig. 4.13). It means that the pixel are working and the problem is related to the parallel readout. Copper trace on the CB\textsuperscript{4C} and Motherboard\textsubscript{Opt} PCBs has been checked for first but without finding anything wrong. Thus the reasons for the blind columns can be addressed either to faulty lines of the parallel bus output drivers, or to wire bonding defects.
An x-ray image reported in fig. 4.17. It depicts the same fuse of the previous images but this time put on a tilted steel slab. The tube output was 0.5 mAs at 35 kVp (Oxford x-ray tube with 100 micron W-anode). The wire inside the fuse is clearly visible.

The following operations are not supported by the Medipix2MXR2 chip (see chapter 1):

8.2.2.6 “Matrix resetting”

The matrix resetting operation resets the matrix configuration. This operation does not requires any data. When the user press the “RESET MATRIX” button the subroutine
“resetMatrix()” \((\text{resetMatrix}(\text{chipID as byte}))\) switches on the chip corresponding to the \text{chipID} parameter and then send the “reset matrix” operation code to the \text{MB}_{opt}.

### 8.2.2.7 “FSR test”

This procedure allows to test the Fast Shift Register of the Medipix2 chip. A 256-bit test stream (e.g. a pseudo-random sequence) is sent to the \text{M}_{DPX}2 FSR and then read back (fig. 4.18). If the input and output strings match then the FSR is working properly. It’s possible to change the active FSR by the “spare FSR” option box on the main control panel.

![Screenshot of the \text{MDPX}2 FSR test. Upper trace shows the input test stream (0xAA) while the lower trace is the output stream [Mar07].](image)

### 8.3 The Device Manager

The \text{Device Manager} is an API DLL provided to communicate with the PLX device drivers. When an API function is called by an application, the API DLL handles the call and translates it to an I/O control message and sends it to the driver. Once the driver completes the request, control returns to the API DLL and then to the calling application.

The \text{Device Manager} of \text{PPCsoft} is a customized API DLL based on the PCI API delivered by PLX Tech. It consists of a library of functions, from which PLX chip-
based PCI boards can be accessed and used. The PCI API provides API function groups, which manage the features of the PLX chip such as DMA access, direct data transfers, and interrupt handling.

### 8.4 The Device Driver

The Device Driver contains the API implementation for the specific PLX chip. It supports and the basic functionality required by all device drivers in a Windows environment. The device driver accesses the PLX chip across the PCI bus by using Windows system calls and is also responsible for handling PCI interrupts from the PLX chip.

Each PLX chip type has an associated driver. A single driver is responsible for all devices in the system containing the PLX chip the driver was written for. The `plx9054.sys` is required to drive the PPC PCI card. After the installation, the driver is started during the boot strap as soon as the Windows Plug&Play Manager detects a device that needs it.

PLX delivers a software tool for drivers customisation. If needed, drivers can be modified to take advantage of specific OEM hardware on a device, or possibly to add functionality, such as additional processing in the Interrupt Service Routine.

---

40 The `PCI9054.sys` device drive is delivered by PLX Tech.
8.5 Communication protocols

The development of PC controlled electronic devices implies both hardware and software aspects. Moreover when programmable logic devices are used a third element, the firmware, has to be considered. Thanks to their flexibility, reconfigurable logics help the development and customization of the communication protocols within the limits imposed by the hardware design. This section describes how the control software interacts with the PPC system (high-level protocol) and how the hardware components of the acquisition chain communicate one between the others (low-level protocol).

8.5.1 High-level protocols

8.5.1.1 The GUI-to-PCI communication

When the software application wants to communicate with the PCI card, the first step is to call to the Driver Manager DLL. The Driver Manager generates a Windows API calls to the Device Driver. Driver manager layer also allocates and retains data buffers in user space. The device driver interacts with the hardware (PCI bridge) by means of read and write operations on the local bus or on the bridge’s configuration registers.

When the user wants to write a control word (on the control bi-directional port of the PCI card), it must call the “PCIWrite” subroutine which takes three parameters which are the base address, offset and data to transmit. Reading from the control port requests the “PCIRead” function which takes the base address and the offset as parameters of the memory location to be read and gives back the received value. The same function is used to read from the readout data port. In the actual design, the control port is mapped on the PCI9054 Local Space 0 (offset 0) while the data port is mapped on the Local Space 1 (offset 0).

The CPLD of the PCI9054 card decodes the address and asserts the GL0 signal if the user is accessing the control port or GL1 if the data port access is requested. GL0 and GL1 signals are asserted until the address bus is set. At the same time the CPLD provides the READY# signal which indicates when data are ready to be read or
written. As soon as the \texttt{READY\#} signal is asserted (low), the fPGA reads the 32-bit data (long-word) from the local bus if the \texttt{LW/R\#} is low or write on the local bus data coming from the control or data ports if \texttt{LW/R\#} is high. Actually the read/write clock is obtained the logical product of the \texttt{READY\#} and \texttt{LW/R\#} signals (see the low-level protocols section below).

When DMA is requested, a different a more complex subroutine is exploited. Its parameters are the base address of the memory location, and the length of the transfer, the type (read or write) and an the handle to the file data where the user wants to store or read data.

\section*{8.5.1.2 The \textit{PCI9054-to-OptHub} communication}

After the system power up or the board global reset, all \textit{OptHub} FIFOs are empty. The control input \texttt{FIFOtx} waits for the data (i.e. the operation code (OC) followed by the operation data (OD), if needed). When the first word is written to the \texttt{FIFOtx} it goes directly to the FIFO output port after three Read Clock (\texttt{FifoRxRclk}) rising edges) and the \texttt{FIFOtx EF\#} flag goes high. As soon as the fPGA detects that the \texttt{FIFOtx} is not more empty, it asserts the \texttt{FIFOtx read enable (FifoTxRen\#)} and the \texttt{TRX data valid (DAV\#T)} signals. The data will be sent to the \textit{Motherboard\textsubscript{O}} through the TRX optical fiber at 40 MHz frequency. As soon as the \texttt{FIFOtx EF\#} flag goes low the \texttt{FifoTxRen\#} and the \texttt{DAV\#R} signals are deasserted by the fPGA.

Some operation requires data back from the \textit{MB\textsubscript{O}} board (e.g., when the user wants to read the ID code of Medipix2 chips). After the operation code has been transmitted to the \textit{MB\textsubscript{O}} board and decoded (see next paragraph), data are sent through the TRX optical fiber. The TRX (\texttt{DAV\#R}) signal goes low and asserts the \texttt{FIFOxWEN\#} on the \texttt{FIFORx}. (An interrupt is generated to inform the control software that the requested data are available). The control software send through the GIO pins the request of data command to the fPGA which assert the \texttt{FIFOxREN\#} signal. The reading clock is generated by the PCI card at each reading cycle.

The fPGA state machine (SM) is usually in an IDLE state, waiting for a new command. The first word transmitted by the user is the operation code. When the OC is written to the FIFO, the Output Ready (\texttt{OR\#}) flag goes LOW. The fPGA SM change state (from IDLE to FETCH), load the OC and switch to the DECODE state. Then the
OC is evaluated: if the operation does not require any further data the SM executes the operation (EXECUTE state) and go back on the waiting state (IDLE). If the operation requires data to be executed, the SM waits for the data are loaded into the input FIFO (LOAD state) and then start reading them (START state) and execute the operation (EXECUTE) until it is completed (END state).

The reading from the input FIFO is allowed during the FETCH and the EXECUTE states, respectively for 1 clock and for n clocks depending on the running operation. Vice versa writing on the input FIFO is always permitted unless the FIFO will become full.

8.5.1.3 The OptHub-to-Motherboard_{opt} communication

After the system power up or board reset, all FIFOs are empty. The input FIFO waits for the operation code (OC) and data (D), if needed to perform the requested operation. When the first word (OC) is written to the input FIFO, it goes directly to the FIFO output port after three Read Clock (FifoRxRCLK) rising edges; subsequent words (D) can be accessed using the Read Enable (FifoRxREN#) signal.

The fPGA state machine (SM) is usually in an IDLE state, waiting for a new command. The first word transmitted by the user is the operation code. When the OC is written to the FIFO, the Output Ready (OR#) flag goes LOW. The fPGA SM change state (from IDLE to FETCH), load the OC and switch to the DECODE state. Then the OC is evaluated: if the operation does not require any further data the SM executes the operation (EXECUTE state) and go back on the waiting state (IDLE). If the operation requires data to be executed, the SM waits for the data are loaded into the input FIFO (LOAD state) and then start reading them (START state) and execute the operation (EXECUTE) until it is completed (END state).

The reading from the input FIFO is allowed during the FETCH and the EXECUTE states, respectively for 1 clock and for n clocks depending on the running operation. Vice versa writing on the input FIFO is always permitted unless the FIFO will become full.
8.5.2 Low-level protocols

Low-level protocol defines how the hardware circuits exchange data and handshakes signals between them. All the PPC system boards are equipped with a programmable logics (e.g. fPGA, CPLD) which have an internal programmable hardware structure. This add an high level of flexibility in the protocol development, test and upgrade procedures.

Configuration code (firmware) of the programmable logics has been written by means of the Verilog hardware description language (HDL). Verilog is a C-like programming language used in the design, verification, and implementation of digital logic chips.

A Verilog design consists of a hierarchy of modules. Modules encapsulate design hierarchy, and communicate with other modules through a set of declared input, output, and bi-directional ports. Internally, a module can contain any combination of net or variable declarations (wire, reg, integer, etc.), concurrent and sequential statement blocks, instances of other modules (sub-hierarchy).

The Verilog source code is transformed (“synthesis” process) into a netlist, a logically-equivalent description consisting only of elementary logic primitives (AND, OR, NOT, flip-flops, etc.). Further manipulations to the netlist (“implementation”) ultimately lead to a bitstream-file which can be downloaded into the programmable logic chip.

The Xilinx’s ISE® Foundation™ 9.2i package and the Parallel Cable IV (PC4) programmer have been used to model the PPC system programmable devices. ISE is an integrated software tool which allows to develop, synthetize, simulate HDL modelling codes for the Xilinx’s programmable chips. The PC4 is the hardware interface between ISE and the programmable chip. It connects to the host PC through the built-in, standard IEEE 1284 DB25 parallel port connector and interfaces the target systems using either a 14-wire or a 7-wire ribbon cable. The PC4 exploits the JTAG protocol to program the fPGA, CPLD and flash PROM.
8.5.3 The PCI9054 firmware

The PCI card holds two programmable logics, one FPGA and one CPLD as described in § 3.4. The FPGA is used as interface between the local data bus and the I/O connectors while the CPLD is used to generate control signals for the FPGA and the SRAM modules.

8.5.3.1 FPGA firmware

At present the FPGA implements the clock generator and the data de-/multiplexing between the 32-bit data local bus and the two programmable header connectors. Only few percent of logic resources are used. The remaining part can be used to implement a pipeline logic for the readout data de-serialization.

The LW/R#, READY# and ADS# signals (Local Bus), and the CS[0:1] (from CPLD) generate the read (RCLK) and write (WCLK) clocks used for data exchange with the outer devices (e.g. motherboard card). The CS[0:1] lines defines the time window available for read/write operation that is the time during which the Local Address Bus (LBA) is asserted. The ADS# signal indicates a valid address on LBA and the start of a new bus access. It is asserted (low) only for the first clock of the bus access.

![Diagram](image)

Fig. 0.120. The chip select CS[0] signal (upper trace, in blue) is asserted when the value on Local Address Bus is between 0 to \text{2000 0000}_\text{16}. The ADS# signal (lower trace, in purple) indicates that a valid address is present on the LAB.

The LW/R# is usually low and should stay low for a read operation or go high for a write operation. In fact, LW/R# goes high also during a read operation as shown in fig. 4.20.
Chapter 4 – Characterization of the PPC imaging system

Fig. 0.121. The LW/R# (upper trace, in blue) and the CS[0] (lower trace, in purple) signals during a write operation (left) and a read operation (right).

In order to warrant the correct setup time to I/O data, the RCLK signal is generated as not (LW/R# & ADS) while the WCLK signal is generated as (LW/R# & notREADY#) as shown in fig. 4.21.

Fig. 0.122. On the left picture the WCLK (upper trace, in blue), LW/R# (middle trace, in acqua), and the READY# (lower trace, in purple) signals during a write operation. On the right picture the RCLK (upper trace, in blue), LW/R# (middle trace, in acqua), and the ADS# (lower trace, in purple) signals during a read operation.

Data are read and write by the PCI bridge when the READY# is asserted so they can be read by the fPGA after a READY# assertion during a write operation and before a READY# assertion during a read operation (fig. 4.22).
Fig. 0.123. The RCLK (upper trace, in blue), LW/RI# (middle trace, in acqua), and the READY# (lower trace, in purple) signals during a read operation. The falling edge of the READY# signal comes after the RCKL rising edge to warrant the data setup time.

Fig. 4.23 shows the propagation delay of a signal transmitted through 0.5 m flat cable from the PCI card (output pin of the FPGA) to the Hub card (input pin of the input driver). The average propagation delay is about 3.8 ns for low-to-high signal steps and 3.4 ns for high-to-low transitions.

Fig. 0.124. Propagation delay measured on the CTRL_OUT0 line. Low-to-high (left) and high-to-low (right) transition are considered. Upper traces are taken at the output pin of the FPGA while the lower traces are taken on the OptHub at the input pin of the input driver.

Figure 4.24 shows an oscilloscope screenshot relative to the Scatter/Gather DMA transfer of 1 KB payload from the PCI card to the PC system memory. The READY# (upper trace) and the ADS# (lower trace) signals are showed. Each low pulse of the ADS# signal states the start of a new address phase to set the base address of the memory location to be read. After that the local memory address is incremented (“burst transfer”). As shown, 1 kB of long-word (32-bit data) is acquired in ~ 7.5 μs
which means an estimated data transfer of about 133 MB/s that is the maximum throughput of the PCI bus.

![Oscilloscope screenshot showing the READY# and the ADS# signal during the DMA acquisition of 1 kB from the PCI card to the PC system memory.](image)

Fig. 0.125. Oscilloscope screenshot showing the READY# and the ADS# signal during the DMA acquisition of 1 kB from the PCI card to the PC system memory.

### 8.5.3.2 CPLD firmware

The CPLD only implements

### 8.5.4 The MotherboardOpt firmware

The board control logic is implemented into the fPGA device manager. The working process is regulated by a finite state machine (FSM) depicted in fig 4.25.

The FSM scheme allows to implement synchronous and asynchronous operation. Synchronous operation have a well-defined life time that is they start and finish in a predefinited numbers of clock cycle. On the contrary the asynchronous operation finishes when the user sent the proper code. The first two state of the FSM are common to all operation. The fPGA is usually in idle state (idle) until a new operation code (OC) is stored into the FIFOrx. The OC is loaded on a dedicated 16-bit internal register (opCode) during the fetch state. The next step consists on the OC decode. If the procedure requires further date (i.e. DACs and matrix settings) the FSM switch to the load state or jumps to the start state. If an asynchronous
operation has been required the FSM switch to the **wait** state until a “stop” OC arrives.

![ FSM Diagram ]

**Fig. 0.126. The FSM scheme implemented into the MB_{opt} FPGA.**

### 8.5.4.1 **Hardware handshake protocol**

The most important part of the firmware is the one that allows the fPGA to acquire the operation code. After that, the state machine can drive the corresponding procedure. This requires a perfect matching between the firmware and the FIFO\_rx communication protocol. The FIFO\_rx is programmed to work in the so-called *First Word Fall Through* (FWFT) mode [DS01]. The first word written into the FIFO goes directly to its output port after three Read Clock (FIFO\_rx\_CLK) rising edges. The IR\# (input ready) and OR\# (output ready) flags are used to indicate that the FIFO\_rx has free space available for writing and that the FIFO\_rx has some data stored into, respectively.

When the first word is written into the FIFO\_tx the IR\# flag goes low. As soon as the fPGA detects that the FIFO\_tx is not more empty, it asserts the FIFO\_tx read enable (FIFO\_tx\_REN\#) and the word is loaded into the fPGA (**fetch** state).

After the first write is performed, the Output Ready (OR\#) flag goes LOW to indicate that there is valid data at the data outputs (Q0-Q15). Subsequent writes will
continue to fill up the FIFOrx until empty space is available. When the FIFOrx is full, the Input Ready (IR#) flag goes HIGH to indicate that there isn’t any free space for writing. When the FIFOrx become full no further write operations are allowed (the FPGA will de-asserts WEN# as soon as IR# is asserted).

After the FIFOrx has stored the incoming data, read operations can start and continue until the FIFOrx become empty. When the last word has been read from the FIFOrx, OR# will go HIGH inhibiting further read operations.

Fig. 0.127. Screenshot of the DACs config operation. Write clock (upper trace) indicates data loading into the input FIFO; read enable strobes (middle trace) indicate data reading from the input FIFO; input ready (IR#) flag (lower trace) indicates if data are available on the FIFO output port.
Chapter 4 – Characterization of the PPC Imaging System

Fig. 0.128. Zoom of the previous screenshot. Progressive actions are numbered to indicate the correct sequence.

Fig. 0.129. Screenshot of the DACs config operation. Write clock (upper trace) indicates data loading into the input FIFO; read enable strobes (middle trace) indicate data reading from the input FIFO; the lower trace indicates the serial data stream sent by the fPGA to the chipboard (cb_sdi line). On left picture is shown the whole operation while the screenshot on the right side is a zoom of the serial stream.
8.6 Summary

In this chapter the control software and the firmware of the PPC readout system has been presented. The use of programmable logic helps the development of the low-level communication protocol giving an high flexibility in modelling the hardware design. The high-level and low-level protocols have been described together with the relative characterization tests.

The system is capable to configure the Medipix2 quad and acquire images through both the serial and the parallel readout. Single DMA acquisitions have been tested too confirming the expected throughput. Sustained DMA acquisition mode is under development; it requires to implement an interrupt handler into the Device Driver.

At present the image data handling (de-serialization and decript) are accomplished by software which slower the image visualization. Further improvements are expected from implementing such a algorithms on hardware (e.g. by the PCI9054 fPGA).
8.6.1 Bibliography

[DS01] Datasheet of IDT72V2113 available at IDT web site www.idt.com

An x-ray imaging acquisition system for digital projection radiography and CT applications has been developed. It consists of three custom-designed electronic boards plus a PCI digital interface card to link the system to the host PC. The imaging system features a reliable optical link to connect the detector stage to the host PC, allowing long, flexible and fast interconnections.

The imaging system exploits a direct-conversion hybrid detector based on the photon counting Medipix2 quad readout chip bump-bonded to a silicon sensor. The active area is segmented in 512 x 512 square pixels with 55 μm side length.

The acquisition chain is controlled by a software developed for test and debug procedures. Fast acquisition mode of images allows to acquire images with a frame rate of 25 frame/s with only 10% of dead acquisition time.

The characterization tests show that the PPC imaging system is working. The system is able to control and configure the detector (Medipix2 and Medipix2mxr20) and raw images have been acquired both with the serial and the parallel readout mode. At present the image data handling (de-serialization and decript) are accomplished by software which slower the image visualization. Further
improvements are expected from implementing such algorithms on hardware (e.g. by the PCI9054 FPGA) and some hardware upgrades as suggested in the text.